
MC

Rev:V2.4

: 2016 10 10

MC

V2.4

2016-10-10

B 5

518057

www.megmeet.com

400-666-2-163

0755-86600999

PLC

PLC

MC

PLC

.....	1
.....	13
.....	38
.....	52
.....	62
.....	77
.....	254
.....	278
.....	288
.....	298

	MC100	MC200	MC280	PLC	
					1
1.1					2
1.1.1	MC	PLC			2
1.1.2	MC80				4
1.1.3	MC100				5
1.1.4	MC200				5
1.1.5	MC280				6
1.2	X_Builder				6
1.2.1					7
1.2.2	X_Builder				7
1.2.3	X_Builder				7
1.2.4					8
1.3					8
1.3.1					8
1.3.2					9
1.3.3					9
1.4					10
1.4.1	Modbus				10
1.4.2	MCbus				10
1.4.3					10
1.5	MC	PLC			10
1.5.1					10
1.5.2	IO				11
1.5.3					12
1.5.4					12
1.5.5					12

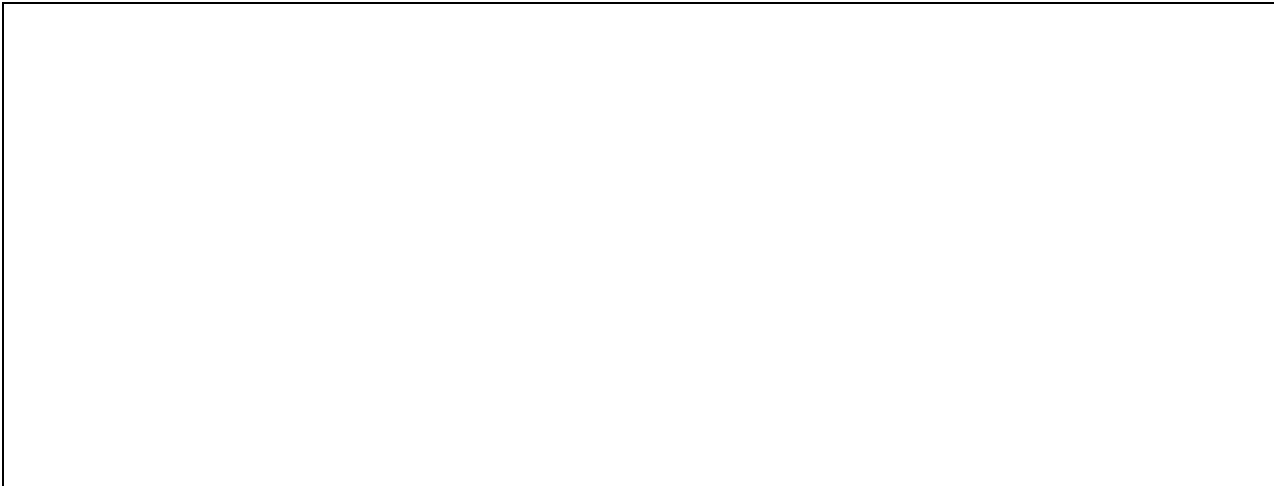
1.1

MC

PLC

		MC280		MC200		MC100		MC80	
		32k	64kByte	12k	24kByte	16k	24kByte	6k	12kByte
		R		C		320		320	180
				200		180			
				1		EEPROM		EEPROM	
		100ms T0 T209 10ms T210 T479 1ms T480 T511		100ms T0 T209 10ms T210 T251 1ms T252 T255					
		16 C0 C199 32 C200 C235 32 C236 C259 C301 C306		16 C0 C199 32 C200 C235 32 C236 C259					
		D0 D7999 R0 R32767		D0 D7999		D0 D7999		D0 D3999	
		V0 V63							
		Z0 Z15							
		SD0 SD511		SD0 SD255					
		M0 M10239		M0 M1999		M0 M2047		M0 M1023	
		LM0 LM63							
		SM0 SM511		SM0 SM255					
		S0 S4095		S0 S991		S0 S1023		S0 S1023	
		3		3		3		3	
		16		16		16		16	
		8		6		6		6	
		12		10		8		4	
	PTO	6		2		2		2	
		3		/		/		/	
		6		/		/		/	
		1		1		1		1	
		0.065 S		0.09 S		0.3 S		0.3 S	
		3		3		100		100	
				2 /8		2 /8			
		PORT0 RS232 PORT1 RS485 PORT2 RS485		PORT0 RS232 PORT1 RS232/RS485		PORT0 RS232 PORT1 RS232/RS485		PORT0 RS232	
		Modbus/	/MCbus/						

		MC280	MC200	MC100	MC80
	,				.9
					DRVI
	IO				PLS
	MODBUS				
	EEPROM				
					PID

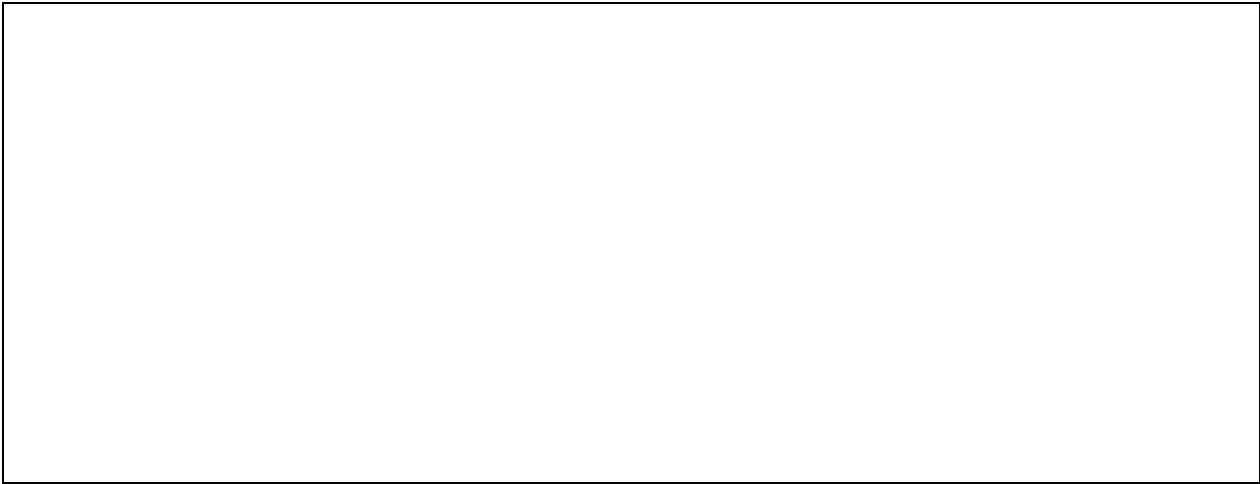


1-1 MC80

PORT0 RS232 Mini DIN8 ON TM OFF

1.1.3 MC100

MC100 MC100-1614BRA



1-2 MC100

PORT0 PORT1 PORT0 RS232 Mini DIN8 PORT1 RS485 RS232
ON TM OFF B II



6

1.2.1

X_Builder

IBM PC

Microsoft Windows

Windows 98 NT 4.0 Windows 2000 Windows XP Windows Vista Windows7

X_Builder

1-2 X_Builder

CPU	Intel	Pentium 233	CPU	Intel	Pentium 1G	CPU
	64M			128M		
	640	480	256	800	600	65535
	DB9		RS232	USB	RS232	USB
	PLC					

1.2.2 X_Builder

X_Builder

Megmeet

X_Builder

Windows

X_Builder

X_Builder

1.2.3 X_Builder



1-5 X_Builder

X_Builder

X_Builder

1.2.4

USB

PLC

RS232

DB9

1.3

MC

MC

MC100

MC200

MC280

1.3.1

1

MCA200-UDM01SL2

MCA200-UDM01



1-6

2

PLC

PLC-



1-7

3

X-builder

PLC

4

PLC

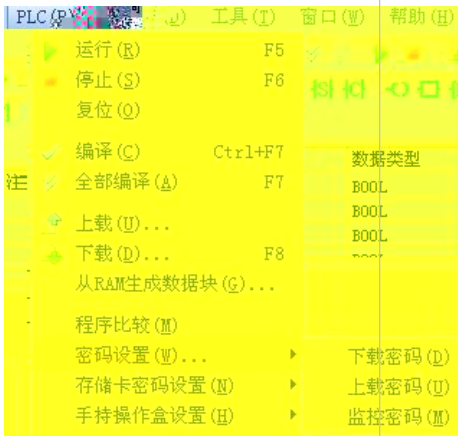
PLC-

PLC

-

/

/



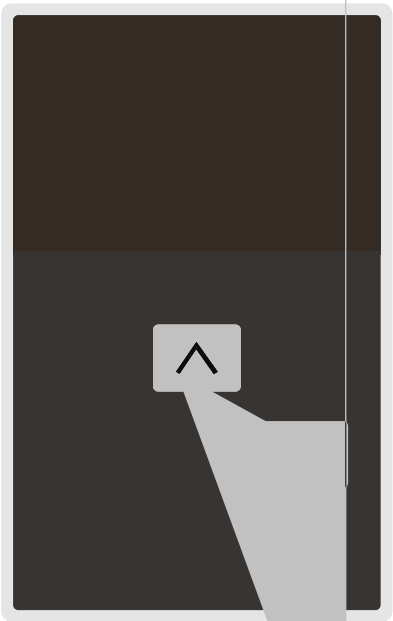
1-8

1.3.2

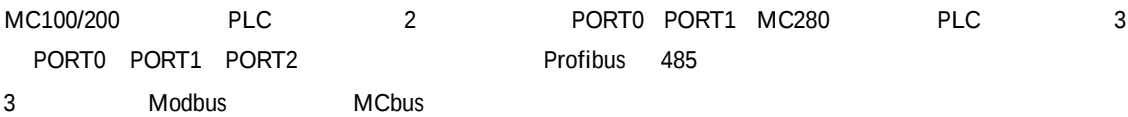
1	MCA200-UDM01SL1	MC	PLC	POWER		
2	UPLOAD	ENT	(WORK)		ERR	
3	DOWNLOAD	WORK		WORK		ERR

1.3.3

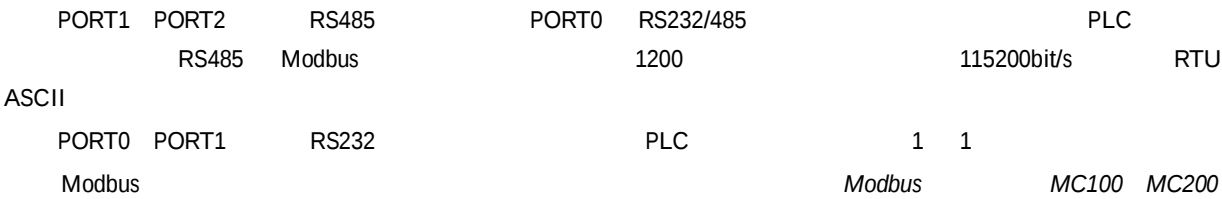
1	MON					
2	PLC	⊖	⊖	SHIFT	ENT	
3		ENT				



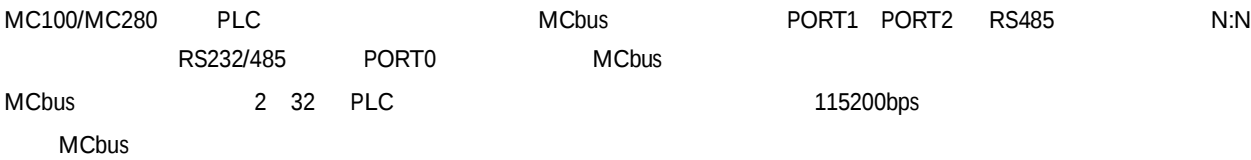
1.4



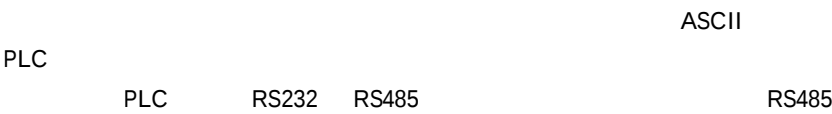
1.4.1 Modbus



1.4.2 MCbus



1.4.3



1.5 MC PLC



1.5.1

MC80	
MC100	

MC200	
MC280	
MC100 (AC)	
MC100 (DC)	

1.5.2 IO

MC100	
MC200	

1.5.3

MC100	
MC200	

1.5.4

MC100	
MC200	

1.5.5

MC200	

	MC	PLC	PLC	
2.1				14
2.1.1				14
2.1.2 PLC				18
2.1.3				19
2.1.4				19
2.1.5				19
2.1.6				19
2.1.7				19
2.1.8 D				20
2.1.9				20
2.1.10				20
2.1.11				21
2.2				21
2.2.1				21
2.2.2				28
2.2.3				29
2.2.4 MC200 MC280 BFM				29
2.3				30
2.3.1				30
2.3.2				30
2.3.3				31
2.4				31
2.4.1				31
2.4.2				31
2.4.3				33
2.4.4				33
2.4.5 PLC				34
2.4.6				35
2.4.7 RAM				36

2.1

2.1.1

2-1 MC100

I/O	I/O	128	
		I/O	4
		16k	
		8000 D	
		0.3 S/	
		S	S /
		32	
		226	
7		128 /128	X0 X177 Y0 Y177 ¹
		2048 M0 M2047	
		64 LM0 LM63	
		256 SM0 SM255	
		1024 S0 S1023	
		256 T0 T255 ²	
		256 C0 C259 ³	
		8000 D0 D7999	
		64 V0 V63	
		16 Z0 Z15	
		256 SD0 SD255	
		16 X0 X7	
		6	
		3	
		8	
	PTO	2	
		1	
		2	0 RS232 1 RS232 RS485
		Modbus	MCbus 1 N N:N
		X0 X1	50kHz X0 X5 80kHz
		X2 X5	10kHz
		Y0 Y1	100kHz
		X0 X7	X0-X3 X4-X7
	⁴	2	
		64	6 16
			3 8
			16
	⁵	X_Builder ⁶	IBM PC
		100	2

2-2 MC80

I/O	I/O	60	
		6k	
		4000 D	
		0.3 S/	
		S S/	
		32	
		200	
7		128 /128 X0 X177 Y0 Y177 ¹	
		1024 M0 M1023	
		64 LM0 LM63	
		256 SM0 SM255	
		1024 S0 S1023	
		256 T0 T255 ²	
		256 C0 C255 ³	
		4000 D0 D3999	
		64 V0 V63	
		16 Z0 Z15	
		256 SD0 SD255	
		16 X0 X7	
		6	
		3	
		4	
	PTO	2	
		1	
		1 0 RS232	
		Modbus	
		X0 X1	50kHz X0 X5 80kHz
		X2 X5	10kHz
		Y0 Y1	50kHz
		X0 X7	
	⁴	2	
		64	6 16
			3 8
			16
	⁵	X_Builder ⁶	IBM PC

2-3 MC200

I/O	I/O	512 256 /256	
		8	8
		12k	
		8000 D	
		0.09 S /	
		S 280 S /	
		32	
		221	
7		256 /256 X0 X377 Y0 Y377 ¹	
		2000 M0 M1999	
		64 LM0 LM63	
		256 SM0 SM255	
		992 S0 S991	
		256 T0 T255 ²	
		256 C0 C255 ³	
		8000 D0 D7999	
		64 V0 V63	
		16 Z0 Z15	
		256 SD0 SD255	
		16 X0 X7 /	
		6	
		3	
		3	
		12	
	PTO	2	
		2 0 RS232 1 RS232 RS485	
		2 485 RS422 RS485	
		Modbus 1 N	
		X0 X1 50kHz X0 X5 80kHz	
		X2 X5 10kHz	
		Y0 Y1 100kHz	
		X0 X17	
	⁴	2	
		64 6	
		16	
			3 8
	⁵	X_Builder ⁶ IBM PC	
		PDA	

2-4 MC280

I/O	I/O	512	256
-----	-----	-----	-----

(2) 10m2 q 8 T 10 T ù f n ù & ù6 ù . ù ù . 0 ù

X_Builder

2.1.4

X_Builder
0



2.1.5

MC200	MC100	MC280
EEPROM		FLASH EEPROM
	FLASH	
RAM		RAM



1		30
2	MC200 MC280 PLC	

2.1.6

PLC STOP RUN EEPROM

2-5 PLC

	OFF → ON	STOP → RUN
EEPROM		
0 0		
0 0		

2.1.7

2-2

MC100
MC200 MC280
MC200

M100 M200
M300 M400

M100 M200 M300 M400



2-2

1	MC200	MC280	PLC	PLC
2	MC100	PLC		

2.1.8 D

MC100	EROMWR	D	D6000	D6999	EEPROM
	2	5ms			
	EEPROM	100	CPU		
	EEPROM				

2.1.9

MC200 X0 X17 MC100 MC280 X0 X17

2.1.10

MC200 MC280

2.1.11

MC100 MC200 MC280 PLC

2-6

	PLC PLC
	/
	/



5	MC	PLC	5
---	----	-----	---

2.2

2.2.1

PLC PLC PLC

•

•
•
•
•
•

PLC/

MC100 MC200 MC280 PLC

SRAM

2-3



2-3



PLC

D M S T C

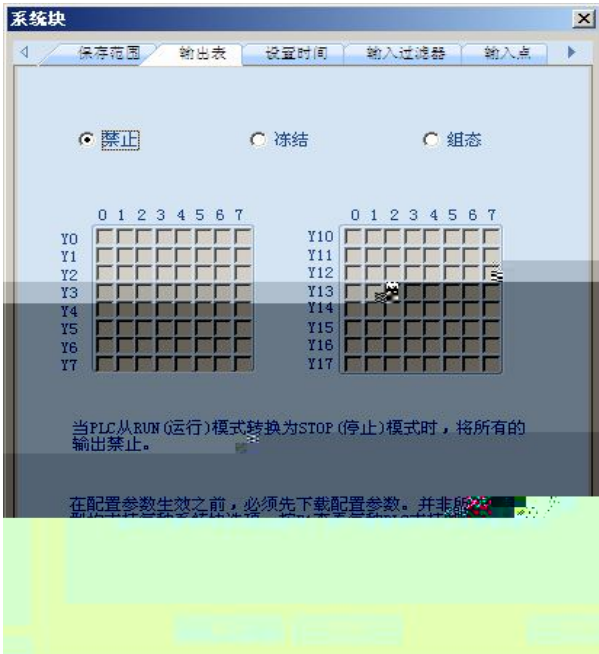
MC200 MC280
MC100



MC100 PLC T

PLC
PLC SRAM SRAM SRAM
SRAM PLC SRAM

PLC 2-4

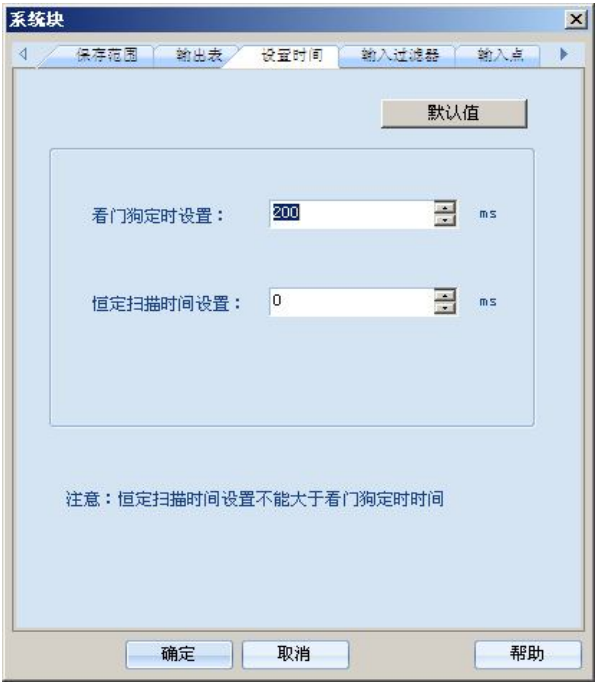


2-4

MC

- CPU
PLC
- (1) PLC
- (2) PLC
- (3) PLC
- 0

2-5



2-5

1.

PLC

1000ms

200ms

0ms

2.

0ms 1000ms 0ms

3.

MC200 MC280

PLC

0ms 100ms 0ms

PLC

MC100

MC280

0 60ms

MC100

X0 X17 MC100 MC280 X0 X17

X0 X3 X4 X7 0 60ms

0 2 4 8 16 32 64

MC200

2-6



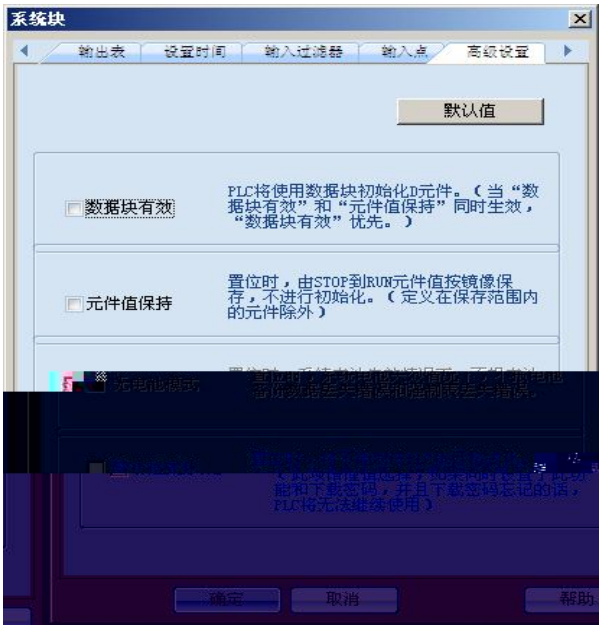
1

STOP

ON



2



2-8

- | | | | | | |
|----|---|-----|------|-----|---|
| 1. | : | PLC | STOP | RUN | D |
| 2. | : | | STOP | RUN | |



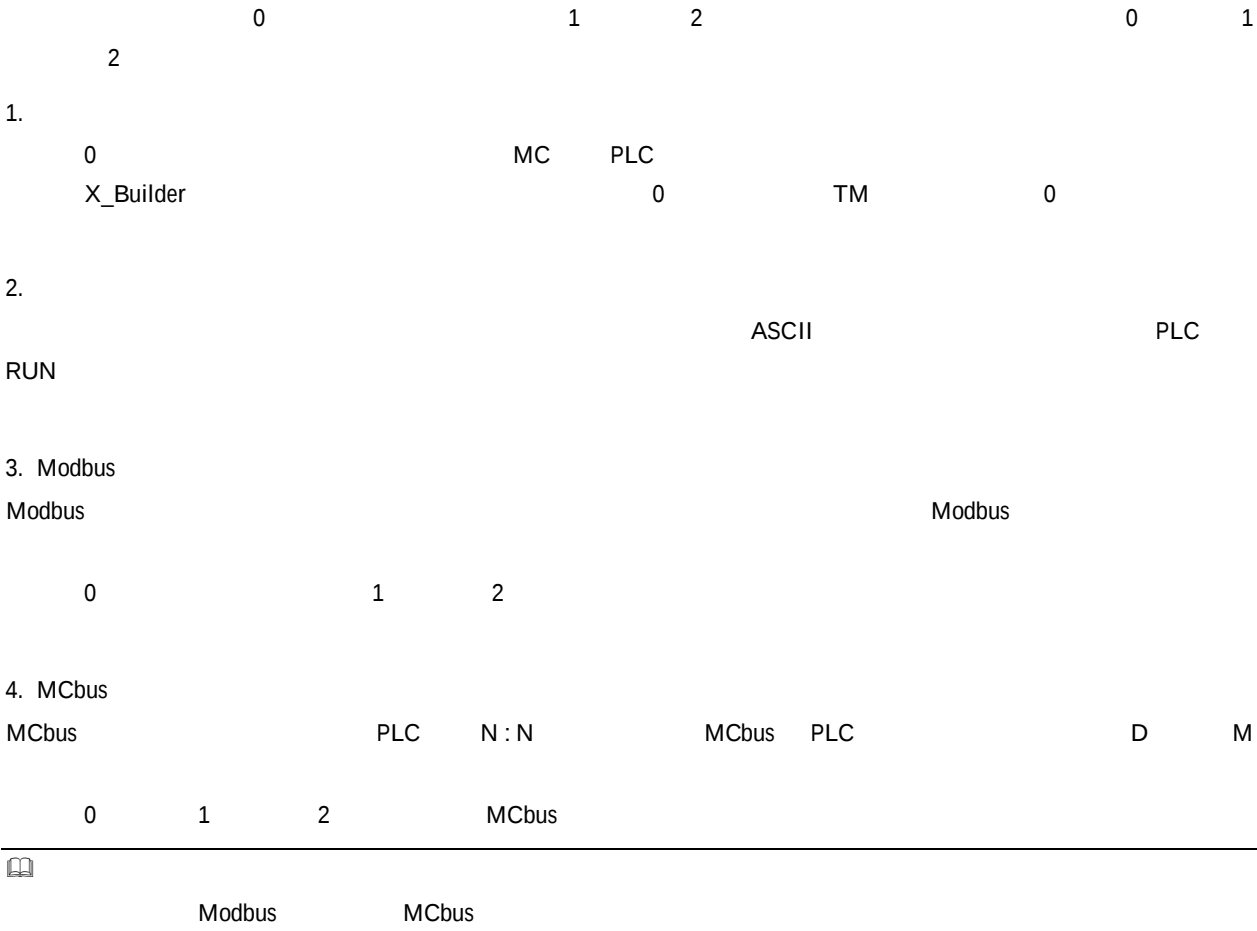
2.1.6

3.

PLC 2 3 2-9

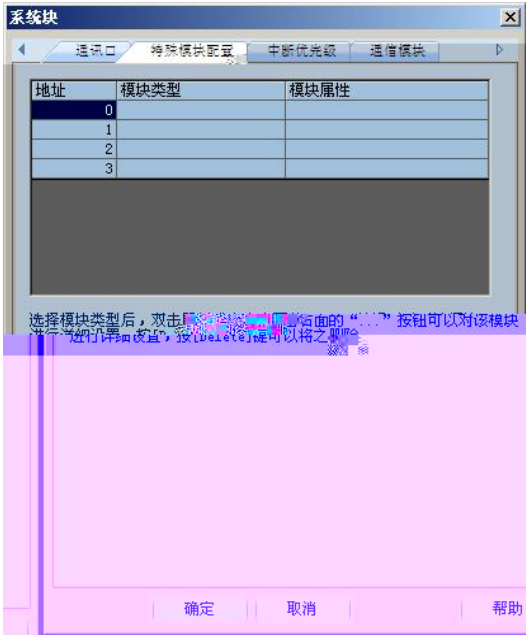


2-9



MC200

2-10



2-10

1.
- 0
- 3

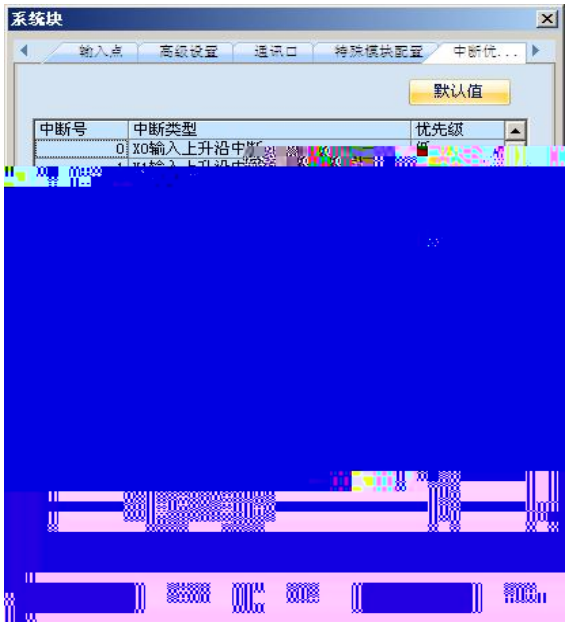
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2-11

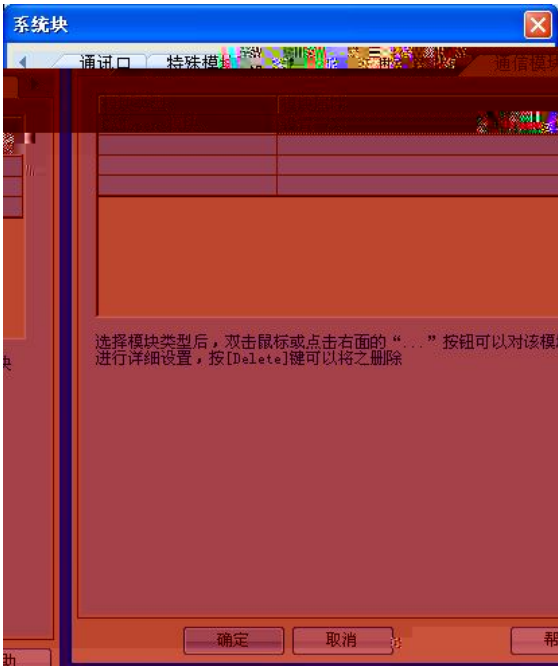
2-12

PLC

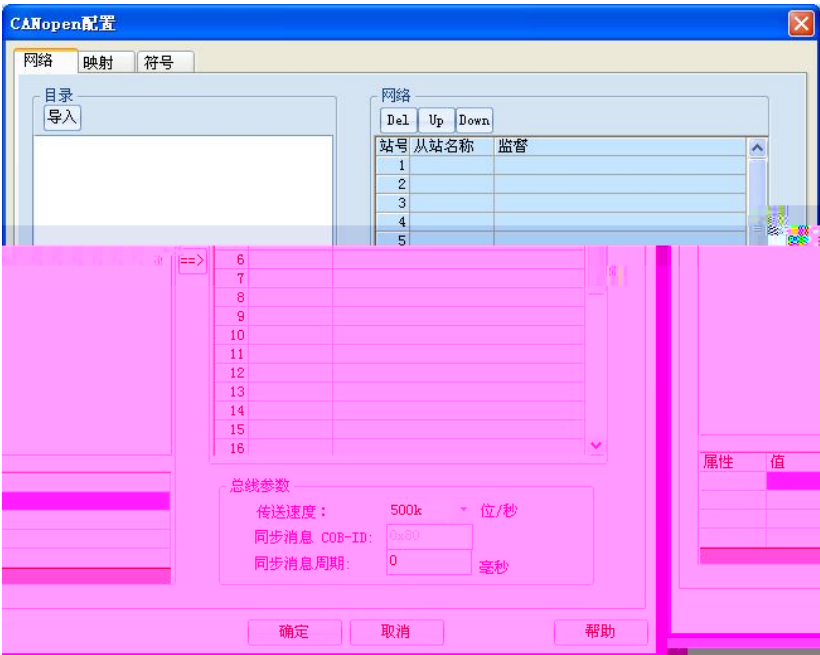


2-12

MC200

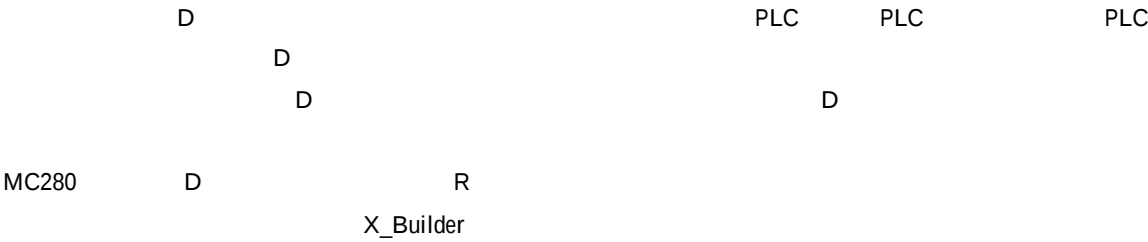


2-13



2-14 CANOPEN

2.2.2



2.2.3

PLC

A Z a z 0 9
8

MC280/100/80

PLC

1000/500/140

2-15

MAIN 全局变量表			
	变量名	变量地址	注释
1	正向定位控制	X4	正向定位控制
2	反向点动	X3	反向点动
3	正向点动	X2	正向点动
4	原点回归	X1	原点回归
5	停止按钮	X0	停止按钮

信息输出

编译 通讯 查找

2-15

2.2.4 MC200 MC280 BFM

MC200 MC280

PLC

MC200 MC280

MC200 MC280

TO

MC200

BFM

MC200

FROM

MC200

BFM

MC200 MC280

MC200 MC280

TO

BFM

MC200

BFM



SD3

SD3

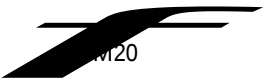
È

P_{SM3}

SD3

ERR

ERR

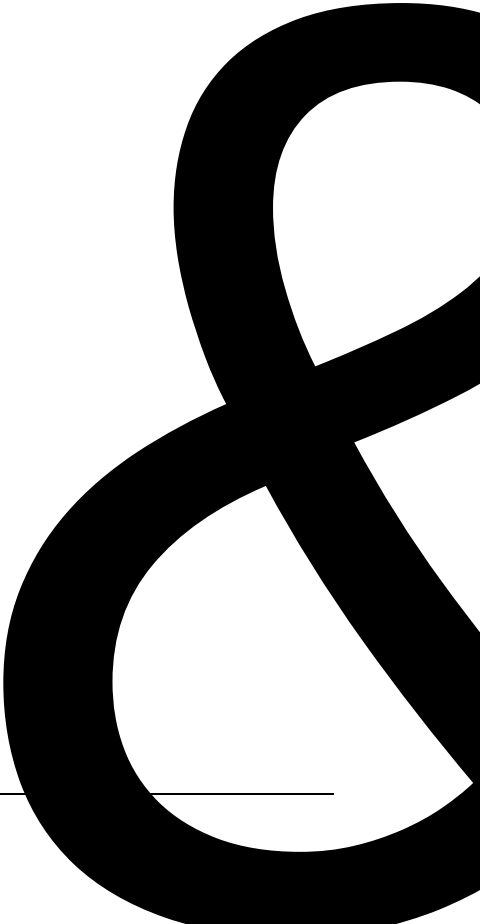
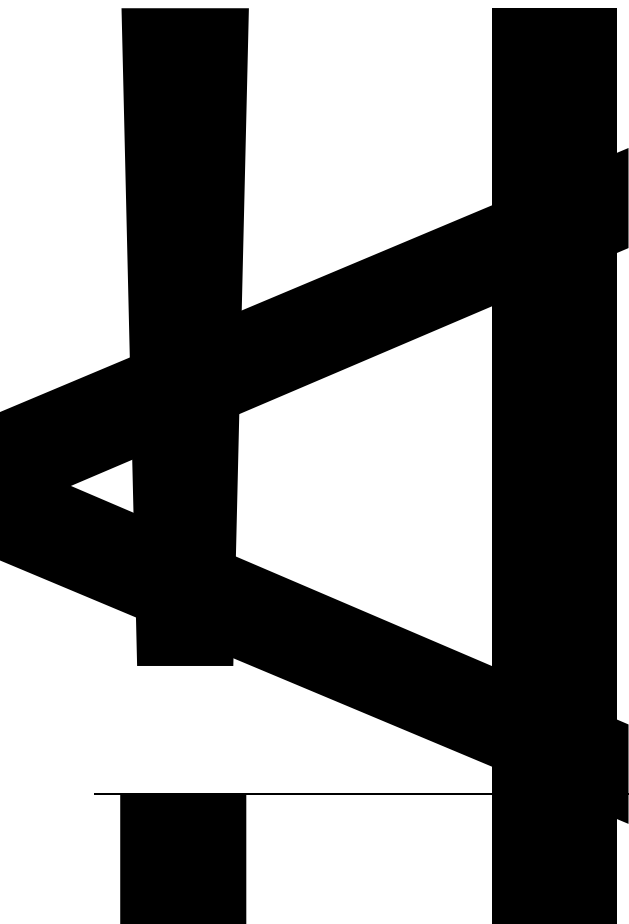


SD20

SM20



SD20





2-19 PLC

SD3

SD20

2.4.3

PLC



PLC

PLC

->

PLC->

PLC

PLC

1

/

2

PLC

2.4.4

PLC

PLC

PLC

PLC

PLC

PLC

PLC

PLC

PLC

PLC



2-21 PLC

PLC

PLC

2.4.6

PLC

PLC

2-22



2-22

2-23



2-23

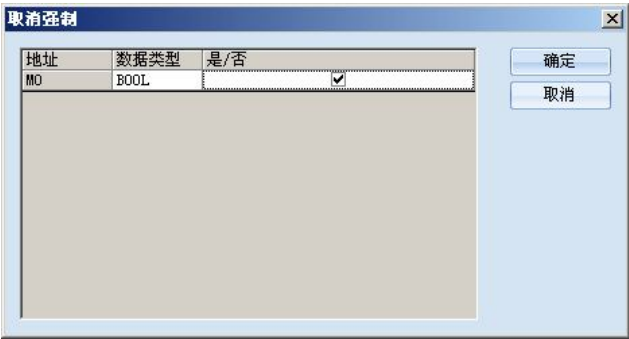
2-24



2-24

PLC

2-25



2-25

PLC

/

2-26



2-26

2.4.7 RAM

PLC D

RAM

2-27

	MC	PLC	
3.1			39
3.1.1			39
3.1.2			40
3.1.3			41
3.1.4			41
3.1.5			42
3.1.6			42
3.1.7			43
3.1.8			43
3.1.9			44
3.1.10			44
3.1.11			45
3.1.12			45
3.1.13			45
3.2			46
3.2.1	.3	Kn	46
3.2.2		Z	46
3.2.3			47
3.2.4	D R V æ. 32	æ.] Ö Ö -	47
3.3			

3.1

3.1.1

PLC

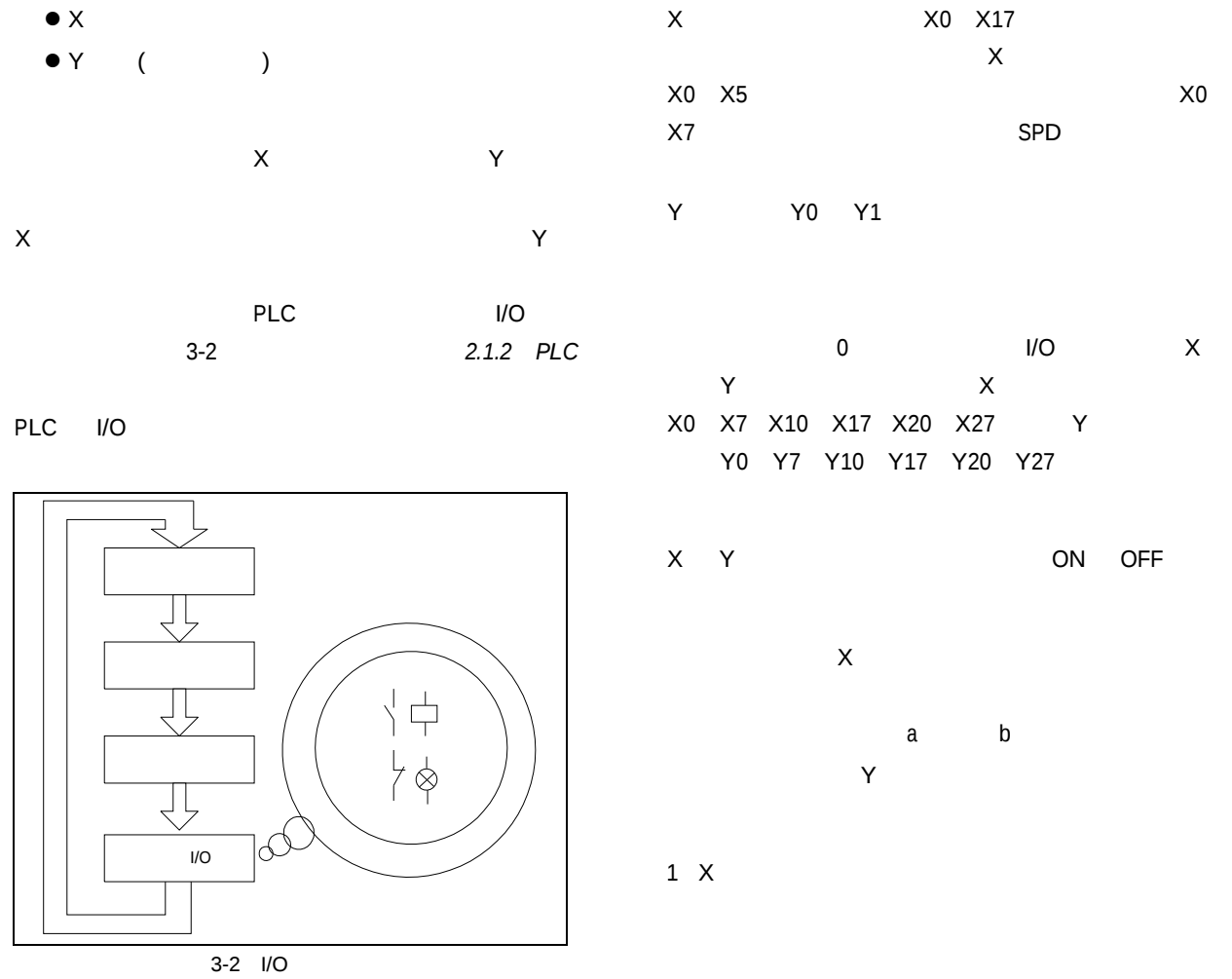
3.1.2

MC PLC
MC PLC

3-1 MC PLC

		MC100	MC200	MC280	
4		128 /128 X0 X177 Y0 Y177 ¹	256 /256 X0 X377 Y0 Y377 ¹	256 /256 X0 X377 Y0 Y377 ¹	8
		2048 M0 M2047	2000 M0 M1999	10240 M0 M10239	10
	5	64 LM0 LM63	64 LM0 LM63	64 LM0 LM63	10
		256 SM0 SM255	256 SM0 SM255	512 SM0 SM511	10
		1024 S0 S1023	992 S0 S991	4096 S0 S4095	10
		256 T0 T255 ²	256 T0 T255 ²	512 T0 T511 ²	10
		256 C0 C255 ³	256 C0 C255 ³	266 C0 C306 ³	10
		8000 D0 D7999	8000 D0 D7999	8000 D0 D7999	10
	R			32768 R0 R32767	10
	5	64 V0 V63	64 V0 V63	64 V0 V63	10
		16 Z0 Z15	16 Z0 Z15	16 Z0 Z15	10
		256 SD0 SD255	256 SD0 SD255	512 SD0 SD511	10
1 X Y 8 X10 8 PLC 2 T (MC80/ MC100/ MC200) ● 100ms T0 T209 ● 10ms T210 T251 ● 1ms T252 T255 (MC280) ● 100ms T0 T209 ● 10ms T210 T479 ● 1ms T480 T511 3 3 C ● 16 C0 C199 ● 32 C200 C235 ● 32 C236 C255 (MC280) ● 16 C0 C199 ● 32 C200 C235 ● 32 C236 C259 C301-C306 C260-C300 4 PLC 5 2					

3.1.3



X

X0 X17

X

X0

X0 X5

X7

SPD

Y

Y0 Y1

0

I/O

X

Y

X0 X7 X10 X17 X20 X27

Y

Y0 Y7 Y10 Y17 Y20 Y27

X Y

ON OFF

X

a b

Y

1 X

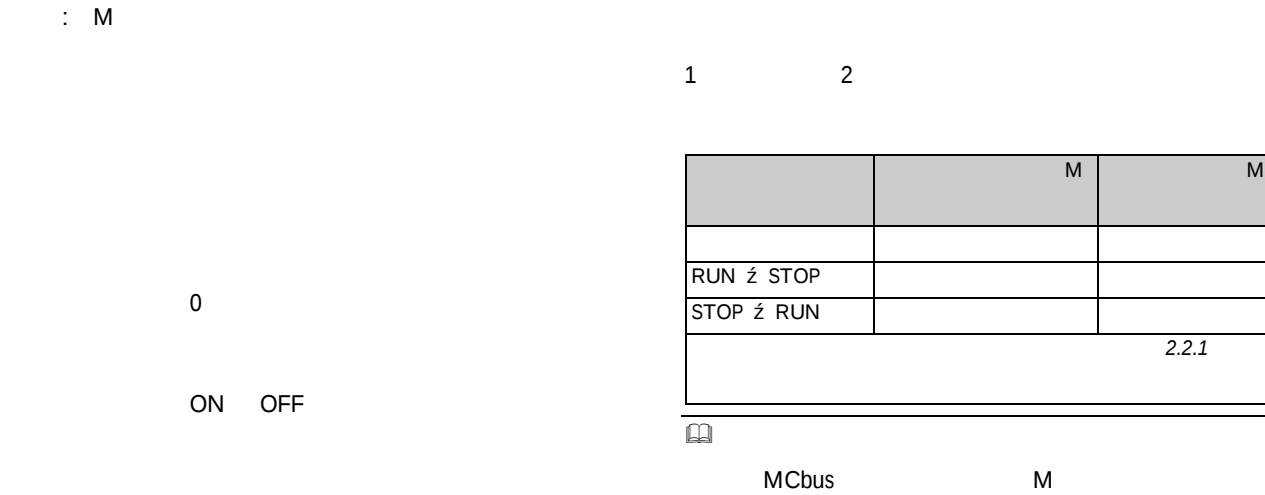
2 Y

3

STOP

Y

3.1.4



3.1.5

S

1

2

STL

M

STL

S

S0 S19

0

ON OFF

	S	S
RUN ě STOP		
STOP ě RUN		
2.2.1		

3.1.6

T

0

T

2

ON OFF

T

16

T

T	1
T	16

3-3 T

T

3

T

T	
T0 T209	
T210 T251	
T252 T255	

1ms T

PLC

10ms 100ms T

PLC

T

4

4

1

2

	T	T
	MC200	
RUN ě STOP		
STOP ě RUN		
2.2.1		

32767

32768

32767

T

T

3.1.7

: C

C

16

C

32

2

C

4

C

C

C

16

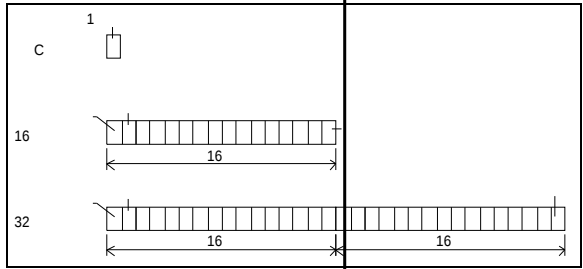
4

32

4

C

C			
C0	C199	16	16
C200	C235	32	32
C236	C259	32	32



3-4 C

16

32

0

ON OFF

æ ĳ ő ȳ € EU& r Qāk ǿ ~ I

MC

3.1.9

SM

SM

PLC
PLC

SM
SM

- SM0 RUN ON
- SM1

3.1.11

:Z

16

3.2.2

Z

Z

Z

0

1

2

3.1.12

LM

0

LM

LM

ON OFF

LM

LM
LM

1

2

4.4

3.1.13

V

0

V

V

ON OFF

V

V
V

1

2

V

4.4

3.2

3.2.1 Kn

Kn

K n U n 1 8 n 4 U

- 1 K1X0 4 X0 X1 X2 X3
- 2 K3Y0 12 Y0 Y01 Y02 Y03 Y04 Y05 Y06 Y07 Y10 Y11 Y12 Y13
- 3 K4M0 16 M0 M1 M2 M3 ě M15
- 4 K8M0 32 M0 M1 M2 M3 ě M31

Kn

Kn

MOV 2#10001001 K2M0 MOV 16#89 K2M0 MOV 137 K2M0 K2M0

K2M0	M7	M6	M5	M4	M3	M2	M1	M0
16#89	1	0	0	0	1	0	0	1

Kn

Kn

DBITS 16# FFFFFFF0 K1M0

2 K1M0

16 1c

16 1c 28

2 K1M0

4

K1M0=16 c 12

3.2.2 Z

MC200/ MC280 PLC Z Z

Z

= Z

D0Z0

Z0=3

D0

Z0

3

D3

Z0=3

MOV 45 D0Z0

MOV 45 D3

D3

45

1

LD M01

MOV 6 Z1

SFTR X0Z1 M0 8 2

LD M0 1

SFTR X6 M0 8 2

Z1=6

X0Z1 = X 0 Z1 = X6

2

LD M0 1

MOV 30 Z20

MOV D100Z20 D0

LD M0 1

MOV D130 D0

Z20=30

D100 Z20 = D 100 Z20 = D130



MOV -30 Z20

MOV D100Z20 D0

MOV D70 D0

2 SM SD

3 Z

D

D7999

Z

D7999Z0

Z0=9

Z

3.2.3

K1X0Z10

Z

Kn

LD M1

MOV 3 Z10

MOV K1X0Z10 D0

LD M1

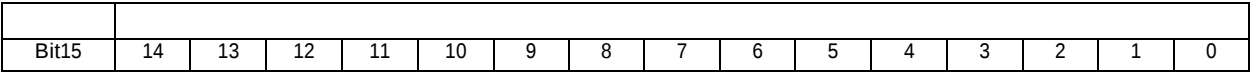
MOV K1X3 D0

Z10=3

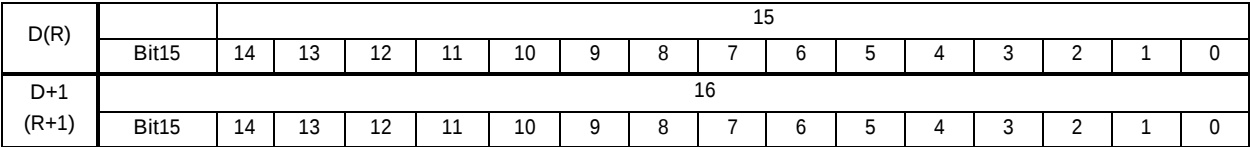
K1X0Z10=K1X 0 Z10 =K1X3

3.2.4 D R V

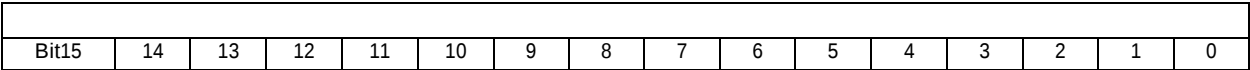
1 INT



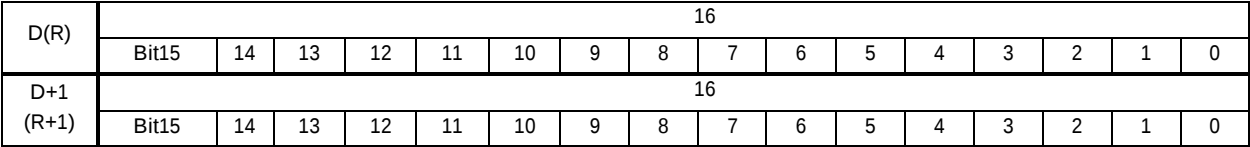
2 DINT



3 WORD



4 DWORD



81632

09A(10)B(11)C(12)D(13)E(14)F(15)

81632248

PLC

0787

100 101 102            
20 21 22            
160 161 162            
80 81 82            

-

-

8Bit11100011

127+126+125+024+023+022+121+120 = 227

-

-

32AC2F

A163+C162+2161+F160 = 44079

PLC

D32bitC

16bitDbit15D

2Dbit31D

2,147,483,647-32,76832,76732bit

01Word7FFF327672Word

7FFFFFFF2,147,483,647

11

MC

PLC

210

a m e a = m | b^e m

d.ddd...dd b e

9.8844 108,

988436216

PLC
32bit

PLC

3.3.2

3-2

BOOL		1	ON OFF 1 0
INT		16	32768 32767
DINT		32	2147483648 2147483647
WORD		16	0 65535 16#0 16#FFFF
DWORD		32	0 4294967295 16#0 16#FFFFFFFF
REAL		32	1.175494E-38 3.402823E 38 ¹

X-builder

a.

7

E-6

ó

E6

ô

X-builder

-E6

-E-6

b.

E-6

E+6

E6

-E-6

X-builder

7

ó

ô

6

3.3.3

3-3

BOOL										C	T			
	X	Y	M	S	LM	SM								
INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

3.3.4

MC200 PLC
3-4

16	8949	32768 32767	
16	65326	0 65535	
32	2147483646	2147483648 2147483647	
32	4294967295	0 4294967295	
16	16#1FE9	16#0 16#FFFF	
32	16#FD1EAFE9	16#0 16#FFFFFFFF	
16	8#7173	8#0 8#177777	
32	8#71732	8#0 8#3777777777	
16	2#10111001	2#0 2#1111111111111111	
32	2#101110011111	2#0 2#1111111111111111 1111111111111111	
	3.1415E-16 3.1415E 3 0.016	1.175494E-38 3.402823E 38	IEEE-754 7

	MC	PLC	
4.1			53
4.1.1	LAD		53
4.1.2	IL		54
4.1.3	SFC		54
4.2			55
4.2.1			55
4.2.2			55
4.2.3			55
4.3			55
4.3.1			55
4.3.2			56
4.4			58
4.4.1			58
4.4.2			58
4.4.3			58
4.4.4			59
4.4.5			59
4.5			61
4.5.1			61
4.5.2			61
4.5.3			61

4.1

LAD

IL

SFC

4.1.1

LAD

PLC

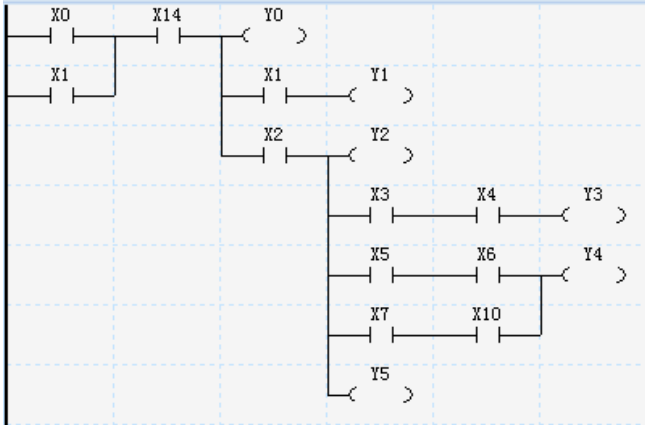
PLC

1

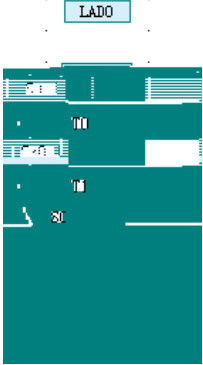
2

4.1.2 IL

PLC

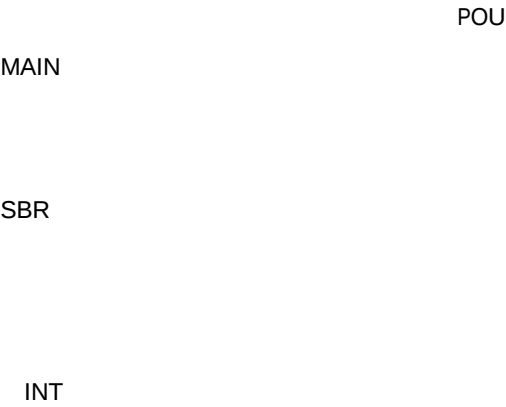
		LD X0
		OR X1
		AND X14
		MPS
		OUT Y0
		AND X1
		OUT Y1
		MPP
		AND X2
		MPS
		OUT Y2
		AND X3
		AND X4
		OUT Y3
		MRD
		LD X5
		AND X6
		LD X7
		AND X10
		ORB
		ANB
		OUT Y4
		MPP
		OUT Y5

4.1.3 SFC

<pre>/*用户程序运行第一个周期，激活S0步进状态*/ SM1 [SET S0] /*步进状态S0的处理*/ S0 < S > Y0 M0 [SET S20] /*步进状态S20的处理*/ S20 < S > Y1 M1 S0 [RET]</pre>	
--	---

4.2

4.2.1



4.2.2

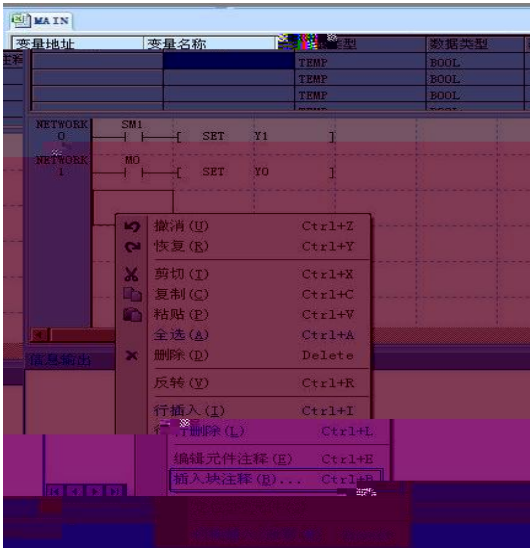


4.2.3

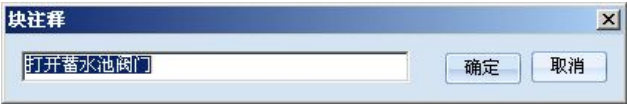


4.3

4.3.1

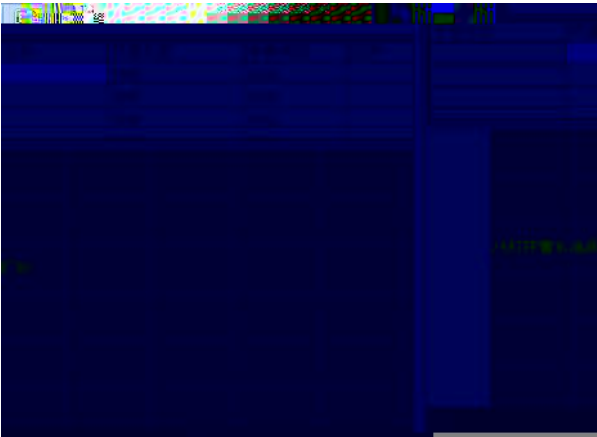


4-4



4-5

/* */

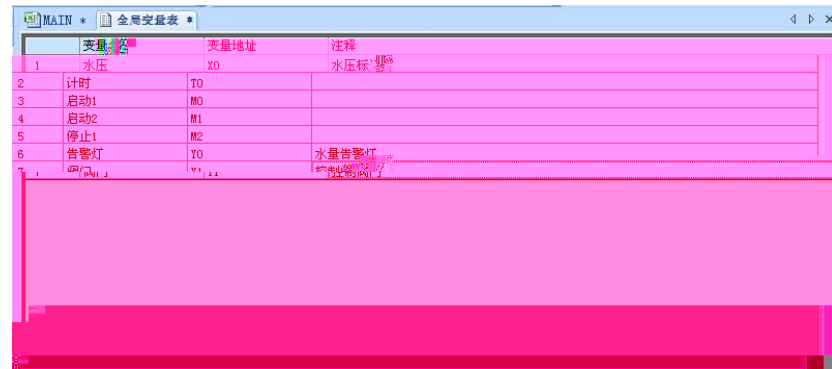


4-6

4.3.2

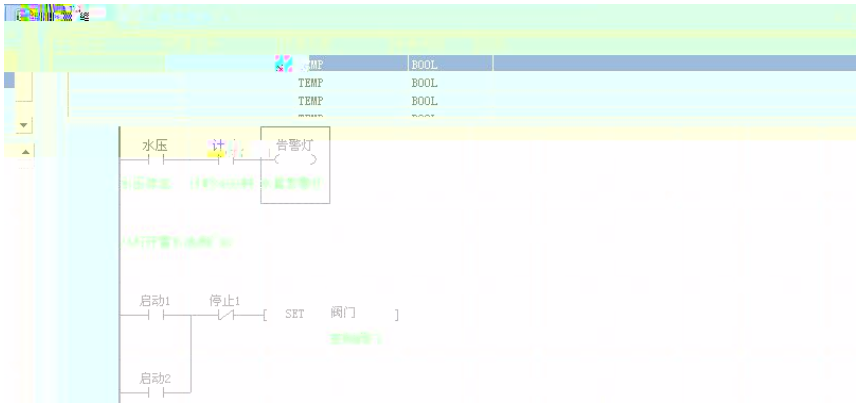
2.2.3

4.4.3



	变量	变量地址	注释
1	水压	X0	水压标志
2	计时	T0	
3	启动1	M0	
4	启动2	M1	
5	停止1	M2	
6	告警灯	T0	水量告警灯

4-1~ y/ TM~ v-b^ •~ ' Ÿ TM€ 'if(€ ``Q~ ¿g'ð TM€ (%of(€y€1~ Gý+^ a bD 7'ð TM€ 'C&(€ 7



4-10



MC200 MC280

PLC

4.4

4.4.1

- 1
- 2
- 3

4.4.2

```
1                                     6
                                     6
MAIN SBR1 SBR2 SBR3 SBR4 SBR5 SBR6
CALL
2
● MAIN SBR0 SBR0
● MAIN SBR0 SBR1 SBR0
3                                     64
4                                     16      16
5                                     CALL
6
```

4.4.3

1				LM	V
2					
3					
		IN	OUT	IN_OUT	TEMP
	● IN				
	● OUT				
	● IN_OUT				
	● TEMP				
4					
				4-1	

4-11 SBR_1

MAIN *SBR_1 *

变量地址	变量名称	变量类型	数据类型	注释
V0	IN1	IN	INT	
V1	IN2	IN_OUT	INT	
		OUT	BOOL	
V2	OUT1	TEMP	INT	
		TEMP	BOOL	

S0

[ADD V0 V1 V2]

3

CALL SBR_1

```
LD M0
CALL SBR_1 3 2 D0
```

- IN1 3
- IN2 2
- OUT1 D0

4.5

4.5.1

●	S	1	S ₁	S ₂	S ₃
●	D	1	D ₁	D ₂	

4.5.2

SM180

SM181

SM182

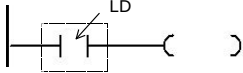
4.5.3

	SPD	X0	X7	
	1			
Modbus	XMT	1		RCV

	MC	PLC	
5.1			63
5.1.1 LD			63
5.1.2 LDI			63
5.1.3 AND			64
5.1.4 ANI			64
5.1.5 OR			64
5.1.6 ORI			65
5.1.7 OUT			65
5.1.8 ANB			66
5.1.9 ORB			66
5.1.10 MPS			67
5.1.11 MRD			67
5.1.12 MPP			67
5.1.13 EU			68
5.1.14 ED			68
5.1.15 INV			68
5.1.16 SET			69
5.1.17 RST			69
5.1.18 NOP			69
5.2			70
5.2.1 MC			70
5.2.2 MCR			70
5.3 SFC			71
5.3.1 STL SFC			71
5.3.2 SET Sxx SFC			71
5.3.3 OUT Sxx SFC			71
5.3.4 RST Sxx SFC			71
5.3.5 RET SFC			72
5.4			73
5.4.1 TON			73
5.4.2 TONR			73
5.4.3 TOF			74
5.4.4 TMON			74
5.5			75
5.5.1 CTU 16			75
5.5.2 CTR 16			75
5.5.3 DCNT 32			76

5.1

5.1.1 LD

										MC200 MC100 MC80 MC280			
LD										1			
S	BOOL	X	Y	M	S	LM	SM		Dx.y*		C	T	

* MC280

S

ON

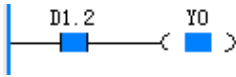
OFF



LD M0

OUT Y0

M0 ON Y0 ON



LD D1.2

OUT Y0

D1 2 1 Y0 ON

MC100

1

MC280

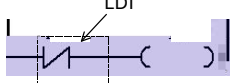
C256 C511 T256 T511 S0 S4096

1 Dx.y 4

M1536 M2047

M1536 M10240

5.1.2 LDI

										MC200 MC100 MC80 MC280			
LDI										1			
S	BOOL	X	Y	M	S	LM	SM		Dx.y*		C	T	

* MC280

S

ON

OFF



LDI M0

OUT Y0

M0 OFF Y0 ON

MC100

1

MC280

C256 C511 T256 T511 S0 S4096

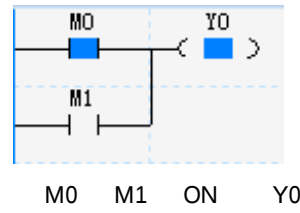
1 Dx.y 4

M1536 M2047

M1536 M10240

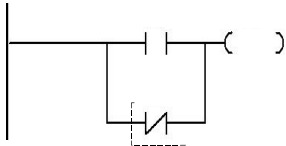
5.1.3 AND

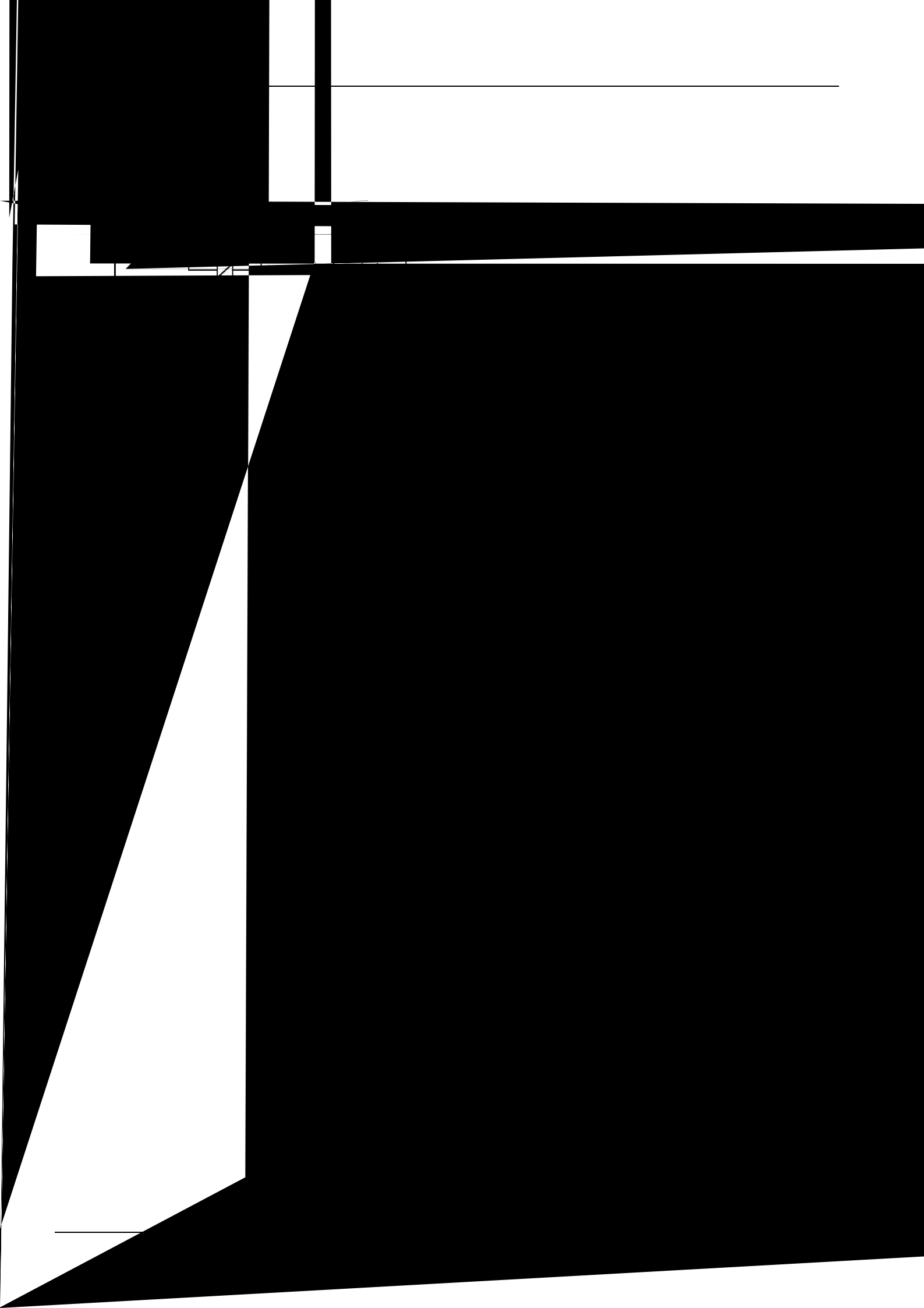
| H | H | H | H | ()

S**S** ON/OFF

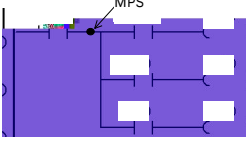
LD M0
 OR M1
 OUT Y0

5.1.6 ORI



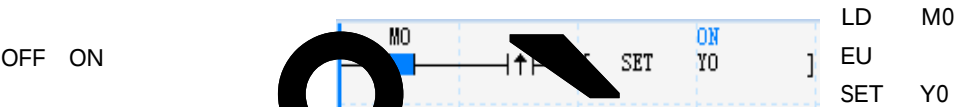


5.1.10 MPS

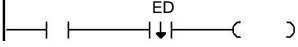
		MC200	MC100	MC80	MC280
MPS		1			

5.1.13 EU

		MC200 MC100 MC80 MC280
EU		2



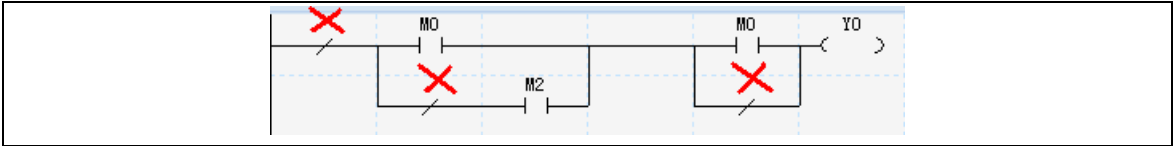
5.1.14 ED

		MC200 MC100 MC80 MC280
ED		2

ON → OFF 0#% j tF Fj M d Å и ħ

INV

INV



5.1.16 SET

				MC200		MC100	MC80	MC280
SET (D)								
SET				1				
S	BOOL		Y	M	S	LM	SM	

S



5.1.17 RST

				MC200		MC100	MC80	MC280
RST (D)								
RST				1				
S	BOOL		Y	M	S	LM	SM	

S



D C

D T

5.1.18 NOP

				MC200		MC100	MC80	MC280
NOP								
NOP				1				

5.2

5.2.1 MC

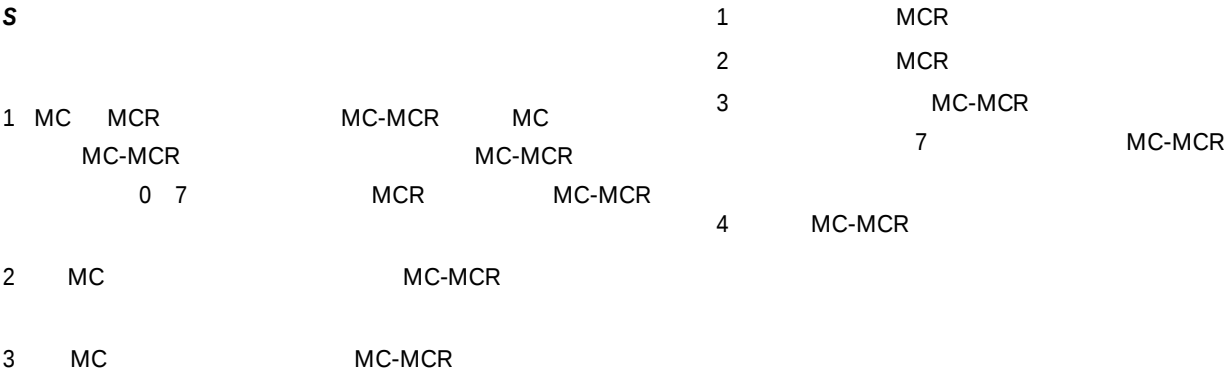
										MC200 MC100 MC80 MC280			
MC										3			
S	INT												

S

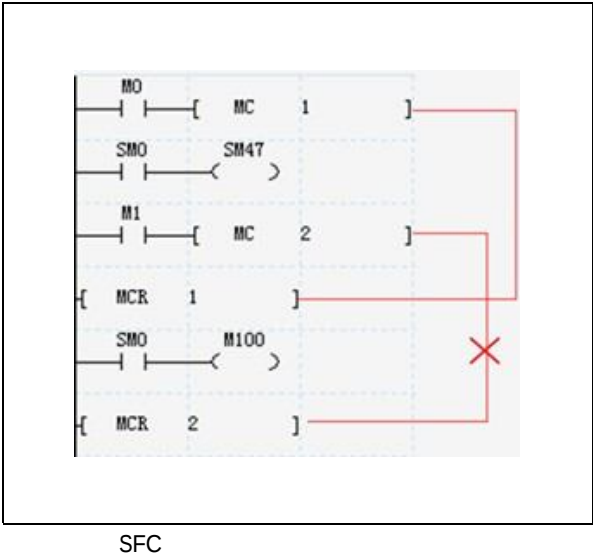
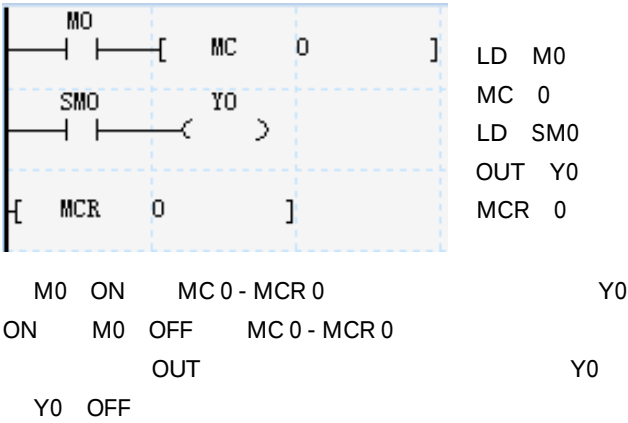
5.2.2 MCR

										MC200 MC100 MC80 MC280			
MCR										1			
S	INT												

S

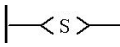


OUT TON TOF PWM HCNT PLSY PLSR DHSCS
SPD DHSCI DHSCR DHSZ DHST DHSP BOUT



5.3 SFC

5.3.1 STL SFC

			MC200	MC100	MC80	MC280
STL			3			
S	BOOL	S				

D

5.3.5 RET SFC

[RET]		MC200 MC100 MC80 MC280
RET		1

5.4

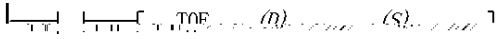
5.4.1 TON

										MC200 MC100 MC80 MC280						
TON D S										5						
D	INT											T				
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	

D
S

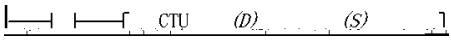
1 32,767 & T
D

5.4.3 TOF

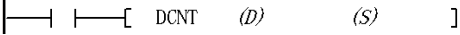
 TOF <i>D</i>		MC200	MC100	MC80	MC280

5.5

5.5.1 CTU 16

 CTU 16		MC200 MC100 MC80 MC280 ° D 0 10	
		5	

5.5.3 DCNT 32

		MC200 MC100 MC80 MC280
DCNT D S		7

	MC	PLC	
6.1			83
6.1.1 FOR			83
6.1.2 NEXT			83
6.1.3 LBL			84
6.1.4 CJ			85
6.1.5 CFEND			85
6.1.6 WDT			86
6.1.7 EI			86
6.1.8 DI			86
6.1.9 CIRET			86
6.1.10 STOP			86
6.1.11 CALL			87
6.1.12 CSRET			87
6.2			88
6.2.1 MOV			88
6.2.2 DMOV			88
6.2.3 RMOV			89
6.2.4 BMOV			89
6.2.5 FMOV			90
6.2.6 DFMov			90
6.2.7 SWAP			91
6.2.8 XCH			91
6.2.9 DXCH			92
6.2.10 PUSH			92
6.2.11 FIFO			93
6.2.12 LIFO			94
6.2.13 WSFR			95
6.2.14 WSFL			96
6.3			97
6.3.1 ADD			97
6.3.2 SUB			97
6.3.3 MUL			98
6.3.4 DIV			98
6.3.5 SQT			99
6.3.6 INC			99
6.3.7 DMC			100
6.3.8 VABS			100
6.3.9 NEG			100

6.3.10	DADD		101
6.3.11	DSUB		101
6.3.12	DMUL		102
6.3.13	DDIV		102
6.3.14	DSQT		103
6.3.15	DINC		103
6.3.16	DDMC		104
6.3.17	DVABS		104
6.3.18	DNEG		105
6.3.19	SUM		105
6.3.20	DSUM		106
6.4			106
6.4.1	RADD		106
6.4.2	RSUB		107
6.4.3	RMUL		107
6.4.4	RDIV		108
6.4.5	RSQT		108
6.4.6	RVABS		109
6.4.7	RNEG		109
6.4.8	SIN	SIN	109
6.4.9	COS	COS	110
6.4.10	TAN	TAN	110
6.4.11	POWER		111
6.4.12	LN	LN	111
6.4.13	EXP		112
6.4.14	RSUM		112
6.4.15	ASIN	ASIN	113
6.4.16	ACOS	ACOS	113
6.4.17	ATAN	ATAN	114
6.4.18	LOG		114
6.4.19	RAD	->	114
6.4.20	DEG	->	115
6.5			116
6.5.2	DTI		116
6.5.3	ITD		117
6.5.4	FLT		117
6.5.5	DFLT		117
6.5.6	INT		118
6.5.7	DINT		118
6.5.8	BCD	16 BCD	119
6.5.9	DBCD	32 BCD	119
6.5.10	BIN	16 BCD	120
6.5.11	DBIN	32 BCD	120
6.5.12	GRY	16	121
6.5.13	DGRY	32	121

6.5.14	GBIN	16		121
6.5.15	DGBIN	32		122
6.5.16	SEG	7		122
6.5.17	ASC	ASCII		123
6.5.18	ITA	16 16	ASCII	123
6.5.19	ATI	ASCII 16 16		124
6.5.20	LCNV			124
6.5.21	RLCNV			125
6.6				127
6.6.1	WAND			127
6.6.2	WOR			127
6.6.3	WXOR			127
6.6.4	WINV			128
6.6.5	DWAND			128
6.6.6	DWOR			129
6.6.7	DWXOR			129
6.6.8	DWINV			129
6.7				130
6.7.1	ROR	16		130
6.7.2	ROL	16		131
6.7.3	RCR	16		131
6.7.4	RCL	16		132
6.7.5	DROR	32		132
6.7.6	DROL	32		133
6.7.7	DRCR	32		133
6.7.8	DRCL	32		134
6.7.9	SHR	16		134
6.7.10	SHL	16		135
6.7.11	DSHR	32		135
6.7.12	DSHL	32		136
6.7.13	SFTR			136
6.7.14	SFTL			137
6.8				138
6.8.1	FROM			138
6.8.2	DFROM			139
6.8.3	TO			140
6.8.4	DTO			141
6.8.5	VRRD			141
6.8.6	REFF			142
6.8.7	REF	I/O		142
6.8.8	EROMWR	EEPROM		143
6.8.9	PR			144
6.8.10	TKY			146
6.9				147
6.9.1	TRD			147

6.9.2 TWR	148
6.9.3 TADD	149
6.9.4 TSUB	150
6.9.5 HOUR	151
6.9.6 DCMP = < > <> >= <=	152
6.9.7 TCMP = < > <> >= <=	153
6.9.8 HTOS	154
6.9.9 STOH	154
6.10 IO	155
6.10.1 HCNT	155
6.10.2 DHSCS	157
6.10.3 DHSCI	158
6.10.4 DHSPI	159
6.10.5 DHSCR	160
6.10.6 DHSZ	161
6.10.7 DHST	162
6.10.8 DHSP	164
6.10.9 SPD	166
6.10.10 PLSY	167
6.10.11 PLSR	168
6.10.12 PLS	170
6.10.13 PLSB	171
6.10.14 PWM	173
6.11	174
6.11.1 PID	174
6.11.2 RAMP	177
6.11.3 HACKLE	178
6.11.4 TRIANGLE	179
6.11.5 ABSD	180
6.11.6 DABSD	181
6.11.7 ALT	182
6.12	182
6.12.1 Modbus	

6.14.4 ENCO		198
6.14.5 BITS	ON	198
6.14.6 DBITS	ON	198
6.14.7 BON	ON	199
6.15		199
6.15.1 BLD	LD	199
6.15.2 BLDI	LDI	200
6.15.3 BAND	AND	200
6.15.4 BANI	ANI	201
6.15.5 BOR	OR	201
6.15.6 BORI	ORI	202
6.15.7 BOUT		202
6.15.8 BSET		203
6.15.9 BRST		203
6.16		204
6.16.1 LD = < > <> >= <=	LD	204
6.16.2 AND = < > <> >=		

6.19.8 STRMOV	228
6.21	229
6.21.1 ZRN	229
6.21.2 PLSV	230
6.21.3 DRV1	231
6.21.4 DRVA	232
6.21.5 ABS	233
6.21.6 DSZR DOG	234
6.21.7 STOPDV	236
6.21.8 LIN	237
6.21.9 CW	239
6.21.10 CCW	240
6.21.11 MOVELINK	242
6.21.12 GEARBOX	243
6.21.13 DRVC	243
6.21.14 CAMTABLE	244
6.21.15 CAMBOX	245
6.22	247
6.22.1 MEAN	247
6.22.2 WTOB	247
6.22.3 BTOW	249
6.22.4 UNI	250
6.22.5 DIS	

6.1

6.1.1 FOR

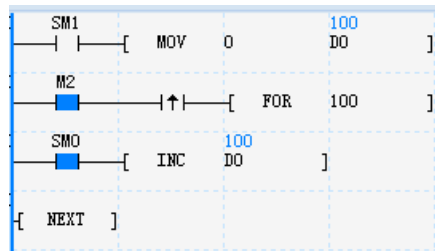
— — [FOR (S)]												MC200 MC100 MC80 MC280					
FOR S												3					
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		

S

6.1.2 NEXT

[NEXT]										MC200 MC100 MC80 MC280			
NEXT										1			

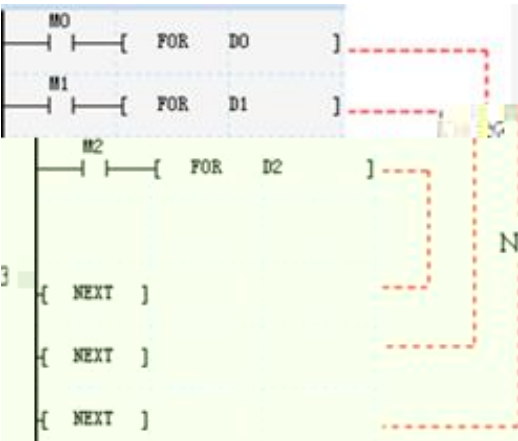
1 FOR NEXT FOR-NEXT
2 FOR FOR-NEXT
3 FOR FOR-NEXT FOR-NEXT



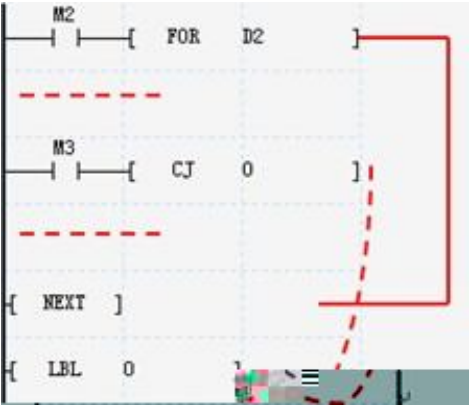
LD SM1
MOV 0 D0
LD M2
EU
FOR 100
LD SM0
INC D100
NEXT

D0=0 M2=OFF M2 OFF ON
FOR-NEXT 100 D0
100 D0=100

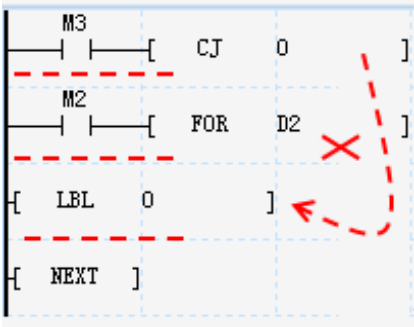
1 FOR-NEXT POU
2 FOR-NEXT MC200 CPU
8 FOR-NEXT
3 FOR-NEXT



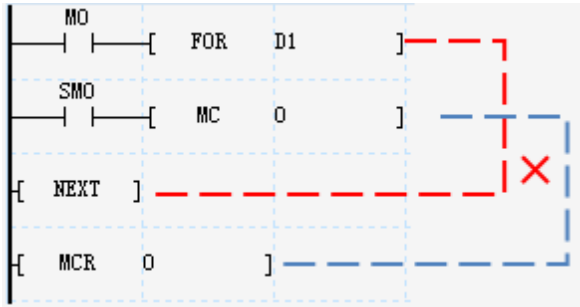
3 CJ



4 CJ



5 MC-MCR FOR-NEXT



FOR-NEXT

WDT

6.1.3 LBL

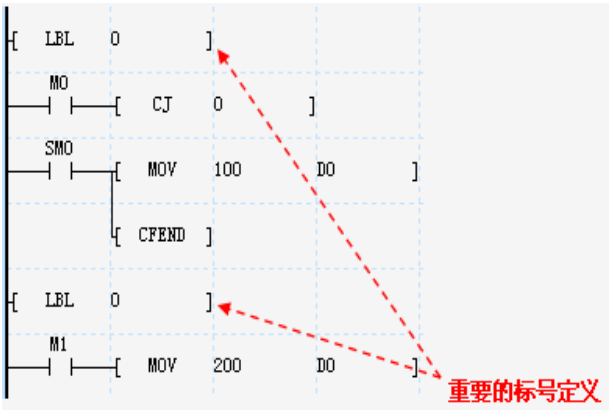
		MC200 MC100 MC80 MC280											
[LBL (S)]													
LBL S		3											
S	INT												

S

1 S
2

1 S 0 S 127
2

CJ



重要的标号定义

6.1.4 CJ

CJ (S)												MC200 MC100 MC80 MC280			
CJ S												3			
S	INT							INT							

6.1.6 WDT

		MC200 MC100 MC80 MC280
WDI		1

6.1.7 EI

MC200 MC100 MC80 MC280

|—| —[EI]

6.1.11 CALL

		MC200	MC100	MC80	MC280
CALL	1	2	ë		

CALL

1 CALL

CALL

2 CALL

SBR1

DINT/DWORD

- CALL SBR1 Z0 Z
 - CALL SBR1 C199 C0 C199
 - CALL SBR1 K2X0 Kn 1 n 3
- SBR1

DINT/DWORD
DINT/DWORD
DINT/DWORD
INT/WORD

- CALL SBR1 C200 C200 C255
- CALL SBR1 K2X0 Kn 4 n 8

INT/WORD
INT/WORD

3 CALL

SBR1

OUT IN_OUT

- CALL SBR1 321
- CALL SBR1 K4X0 K4X0
- CALL SBR1 SD0 SD0

OUT IN_OUT
OUT IN_OUT
OUT IN_OUT

4 CALL

6.1.12 CSRET

		MC200	MC100	MC80	MC280
CSRET		1			

6.2.3 RMOV

										MC200 MC100 MC80 MC280					
RMOV S D										7					
S	REAL								D				V		R
D	REAL								D				V		R

S

D

LD X0

RMOV D0 D10

X0=ON

D0,D1

D10,D11

D10,D11 =5.000050

S

D S

6.2.4 BMOV

										MC200 MC100 MC80 MC280					
BMOV S1 D S2										7					
S1	INT		KnX	KnY	KnM	KnS	KnLM		D	SD	C	T	V		R
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S

D

LD X0

BMOV D0 D100 10

X0=ON

D0 10

D100 10

S2

S1

D

S2

S1

S2

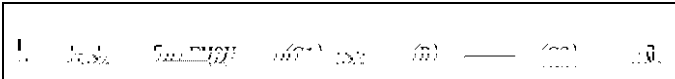
D100=D0

D101=D1

.....

D109=D9

6.2.5 FMOV

										MC200 MC100 MC80 MC280					
FMOV S1 D S2										7					
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1

D

S2

1 S1 D S2 C

2 S2 0

3 S1 D Kn Kn

C0 C199

S1

D

S2

X0

[

FMOV

D0

D100

10

]

LD X0

FMOV D0 D100

10

X0=ON

D0

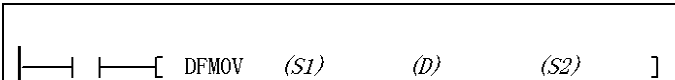
D100

10

D100=D101=

=D109=D0=300

6.2.6 DFMOV

										MC200 MC100 MC80 MC280					
DFMOV S1 D S2										9					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1

D

S2

1 S1 D S2 C

2 S2 0

3 S1 D Kn Kn

C200 C255

S1

D

S2

X0

[

DFMOV

D0

D10

10

]

LD X0

DFMOV D0 D10

10

X0=ON

D0,D1

D10

10

2

D10,D11 =

D12,D13 =

= D28,D29 =

D0,D1 =100000

6.2.7 SWAP

[SWAP (D)]										MC200 MC100 MC80 MC280					
SWAP D										3					
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

X0

[SWAP D0]

LD X0

SWAP D0

X0=ON D0=0x1027 4135

D0 D0=0x2710

D

D

6.2.8 XCH

[XCH (D1) (D2)]										MC200 MC100 MC80 MC280					
XCH D1 D2										5					
D1	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
D2	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

D1

1

D2

2

D1

D2

D1 D2

Kn D1

D2 Kn

1

X0

[XCH D0 D10]

LD XCH

X0=ON D0 D10

D0=5000

D10=1000

D0=1000 D10=5000

2

/*用户人机界面访问D0 D1，对用户来说是可见的*/

/*初始化时记得交换数据位置，使它符合用户人机界面的规则*/

6.2.9 DXCH

6.2.12 LIFO

LIFO (D1) (D2) (S)										MC200 MC100 MC80 MC280					
LIFO D1 D2 S										7					
D1	INT								D				V		R
D2	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

1

S

1

D2

D1

1

2

D1

0

SM180

1

2

D1

3

S

0

M0

LIFO

9

D100

1000

D0

10

LD M0

LIFO D100 D0 10

D0

D110

D109

D108

D107

D106

D105

D104

D103

D102

D101

D100

栈指针

1 M0=ON D110 D0 D101 D110

2 D0=0 D100=10 D101=1000

D102=2000 D109=9000 D110=10000

3 D0=10000 D100=9 D101=1000

D102=2000 D109=9000 D110=10000

6.2.13 WSFR

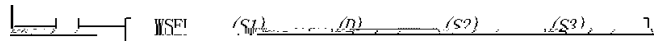
MC200 MC100 MC80 MC280

[WSFR (S1) (D) (S2) (S3)]

6.2.14 WSFL

MC200

C200



6.3

6.3.1 ADD

										MC200 MC100 MC80 MC280				
— — — ADD (S2) (D)														
ADD S1 S2 D										7				
S1	INT		KnY	KnM	KnS	KnLM	M	D	SD	C	T		Z	R
S2	INT		KnY	KnM	KnS	KnLM	M	D	SD	C	T		Z	R
D	INT		KnY	KnM	KnS	KnLM		D		C	T	V		R

S1 1
S2 2
D & Ø £ 1

1 È S1 S2 D
2 D . 32767
SM181 F 1Ç5 Ì 0 SM180
F 1Ç5 È 32767 SM182

X0

[ADD D0 D1 D10]

LD X0
ADD D0 D1 D10
X0=0NB`ëó' D0™1000Ä@•Ä` D1 0 Ä 0
5 D10 D10=60081™C Bie R215

6.3.2 SUB

										MC200 MC100 MC80 MC280						
— — — SUB (S1) (S2) (D)]																
SUB S1 S2 D										7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R	

6.3.3 MUL

										MC200 MC100 MC80 MC280						
MUL S1 S2 D										8						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R	

S11

S22

D

MUL32

S1S2

D

X0

[MULD0D1D10]

LD X0

MUL D0 D1 D10

X0=ON D0 1000 D1 2000

D10,D11 D10,D11 =2000000

6.3.4 DIV

DIV (S1) (S2) (D)												MC200 MC100 MC80 MC280					
DIV S1 S2 D												7					
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R		

S11

S22

D

S200

0

S1S2

D D

X0

[DIVD0D1D10]

LD X0

DIV D0 D1 D10

X0=ON D0 2500 D1 1000

D10,D11 D10=2 D11=500

6.3.5 SQT

[SQT (S) (D)]										
SQT S D										
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD
D	INT			KnY	KnM	KnS	KnLM		D	

S
D

S 0

1

S

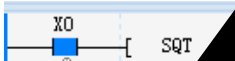
D

2

D

0

SM180



X0=ON

SM182

6.3.6 INC

[INC (D)]										MC200 MC100 MC80 MC280
INC D										
										3
D	INT		KnY	KnM	KnS	KnLM			D	C T V Z R

6.3.7 DMC

										MC200 MC100 MC80 MC280					
															
DMC D										3					
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

D

-32768 32767

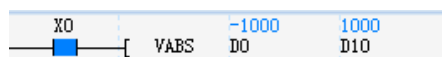
D 1

X0=ON D0 1000 1

LD X0
DMC D0
D0=999

6.3.8 VABS

										MC200 MC100 MC80 MC280					
															
VABS S D										5					
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

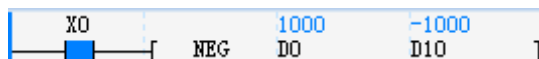
S**S** -32767 32767 **S** -32768**D****S**
D

X0=ON D0 -1000

LD X0
VABS D0 D10
D10 D10=1000

6.3.9 NEG

										MC200 MC100 MC80 MC280					
															
NEG S D										5					
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

S**S** -32767 32767 **S** -32768**D****S**
D

X0=ON D0 1000

LD X0
NEG D0 D10

D10 D10=-1000

6.3.10 DADD

										MC200 MC100 MC80 MC280					
DADD S1 S2 D										10					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R

S1 1
S2 2
D

LD X0
 DADD D0 D2 D10
 X0=ON D0,D1 100000 D2,D3
 200000 D10,D11 D10,D11
 =300000

1 **S1 S2 D**
 2 **D** 2147483647
 SM181 0
 SM180 2147483648
 SM182

6.3.11 DSUB

										MC200 MC100 MC80 MC280					
DSUB S1 S2 D										10					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R

S1 1
S2 2
D

LD X0
 DSUB D0 D2 D10
 X0=ON D0,D1 100000 D2,D3
 200000 D10,D11 D10,D11
 100000

1 **S1 S2 D**
 2 **D** 2147483647
 SM181 0
 SM180 2147483648
 SM182

6.3.12 DMUL

										MC200 MC100 MC80 MC280				
DMUL S1 S2 D										10				
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V	R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D					

6.3.14 DSQT

[DSQT (S) (D)]												MC200 MC100 MC80 MC280					
DSQT S D												7					
S	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R		
D	DINT			KnY	KnM	KnS	KnLM				C		V		R		

S

D

S 0

1

2

S

D

0

SM180

SM182

X0

DSQT

83000D0

288D10

LD X0

DSQT D0 D10

X0=ON

D0,D1

Ä83000

D10,D11

D10,D11

=288

6.3.15 DINC

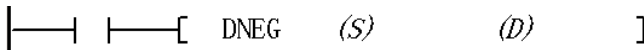
										MC200 MC100 MC80 MC280				
DINC D										4				
D														

D

6.3.16 DDMC

DDEC (D)		MC200	MC100	MC80	MC280

6.3.18 DNEG

												MC200 MC100 MC80 MC280					
DNEG S D												7					
S	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R		
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R		

S

D

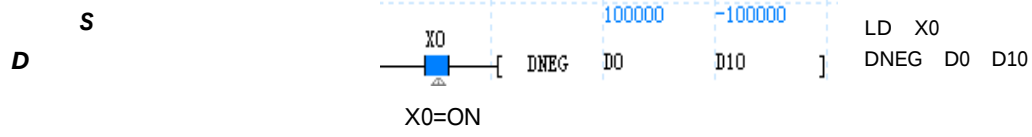
S

2147483647

2147483647

S

2147483648



6.3.20 DSUM

DSUM										MC200				MC100		MC80		MC280			
DSUM										S1		S2		D		9					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R						
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R						
D	DINT			KnY	KnM	KnS	KnLM		D		C		V		R						

S1

S2

D

S1

S2 2

D

SM0

[DMOV 100000 D0]

[DMOV 200000 D2]

[DMOV 300000 D4]

[DMOV 400000 D6]

[DMOV 500000 D8]

X0

[DSUM D0 5 D100]

LD SM0

DMOV 100000 D0

DMOV 200000 D2

DMOV 300000 D4

DMOV 400000 D6

DMOV 500000 D8

LD X0

DSUM D0 5 D100

0 S2 255

X0=ON D0 5 2

D100,D101

D100,D101 = D0,D1 D8,D9 =1500000

6.4

6.4.1 RADD

[RADD (S1) (S2) (D)]											MC200 MC100 MC280					
RADD S1 S2 D											10					
S1	REAL								D				V		R	
S2	REAL								D				V		R	
D	REAL								D				V		R	

SM181

0

SM180

S1

1

S2

2

D

X0

[RADD D0 -1000.20 D2 2000.500 D10 1000.300]

LD X0

RADD D0 D2 D10

1

S1

S2

D

2

D

X0=ON D0,D1 -1000.20 D2,D3 2000.500

D10,D11 D10,D11 =-1000.300

1.701412e 038

1.701412e 038

6.4.2 RSUB

										MC200 MC100 MC280						
RSUB S1 S2 D										10						
S1	REAL								D				V		R	
S2	REAL								D				V		R	
D	REAL								D				V		R	

S1 1
S2 2
D

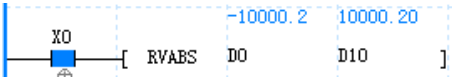
1

6.4.4 RDIV

6.4.6 RVABS

		[RVABS (S) (D)]										MC200 MC100 MC280		
		RVABS S D										7		
S	REAL								D				V	R
D	REAL								D				V	R

S
D



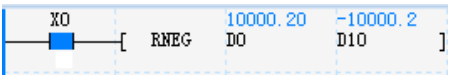
S D

LD X0
RVABS D0 D10
X0=ON D0,D1 -10000.2
D10,D11 D10,D11 =10000.2

6.4.7 RNEG

		[RNEG (S) (D)]										MC200 MC100 MC280		
		RNEG S D										7		
S	REAL								D				V	R
D	REAL								D				V	R

S
D



S D

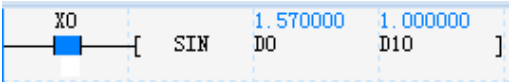
LD X0
RNEG D0 D10
X0=ON D0,D1 =10000.2
D10,D11 D10,D11 -=10000.2

6.4.8 SIN SIN

		[SIN (S) (D)]										MC200 MC100 MC280		
		SIN S D										7		
S	REAL								D				V	R
D	REAL								D				V	R

2 D 0 SM180

S
D



1 S SIN
D

LD X0
SIN D0 D10

6.4.11 POWER

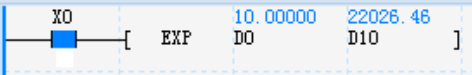
 [POWER (S1) (S2) (D)]													MC200 MC100 MC280				
POWER S1 S2 D													10				
S1	REAL								D				V		R		
S2	REAL								D				V		R		
D	REAL								D				V		R		

6.4.13 EXP

[EXP (S) (D)]												MC200 MC100 MC280						
EXP S D												7						
S	REAL								D				V		R			
D	REAL								D				V		R			

S

D



LD X0

EXP D0 D10

X0=ON

D0,D1 =10.0

EXP

D10,D11

D10,D11

1

S

EXP

=22026.464844

2

D

1.701412e 038

1.701412e 038

SM181

0

SM180

6.4.14 RSUM

RSUM									MC200 MC100 MC280							
RSUM S1 S2 D									9							
S1	REAL								D				V		R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D				V		R	
D	REAL								D				V		R	

S1

S2

D

S1

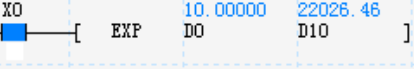
S2 2

D

1 0

S2 255

X0



6.4.15 ASIN

6.4.17 ATAN ATAN

										MC280				
ATAN (S) (D)										7				
S	REAL								D				V	R
D	REAL								D				V	R

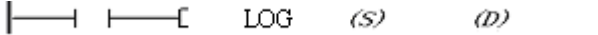
2 D 0 SM180

S
D



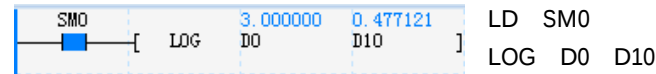
1 S
TAN-1 D SM0=ON (D0 D1) 3.14 TAN-1 (D10 D11) (D10 D11)=1.262481

6.4.18 LOG

										MC280				
LOG (S) (D)										7				
S	REAL								D				V	R
D	REAL								D				V	R

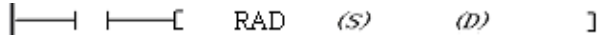
2 D SM181
0 SM180

S
D

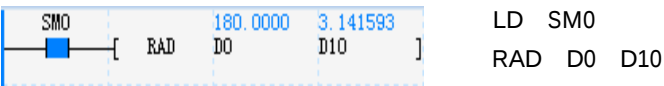


1 S LOG
D LOG 10 SM0=ON D0(D1) 3.0 D10(D11) D10(D11)=0.477121

6.4.19 RAD ->

										MC280				
RAD (S) (D)										7				
S	REAL								D				V	R
D	REAL								D				V	R

S 1 S D
D 2 0 SM180



SM0=ON D0(

6.4.20 DEG ->

			MC280
DEG (S) (D)			7
S	REAL	D	

6.5

				LM/V
BOOL		1	ON OFF	1 LM
INT		16	-32768 +32767	1 V
DINT		32	-2147483648 +2147483647	2 V
WORD		16	0 65535	1 V
DWORD		32	0 4294967295	2 V
REAL		32	Ó1.175494351 E - 38 ~ Ó3.402823466 E + 38	2 V

BCD

-- BCD Binary Coded Decimal
BCD 8421BCD
8421BCD

BCD

	8421BCD	
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	1110
6	0110	1010
7	0111	1000
8	1000	1100
9	1001	0100

6.5.1 DTI

[DTI (S) (D)]												MC200 MC100 MC80 MC280					
DTI S D												6					
S	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R		
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R		

S S 32767 S -32768 D

S D

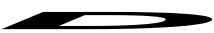
X0	[DTI 10000 D0 10000 D10]
----	----------------------------

X0=ON D0, D1 =10000 D10 D10=10000

LD X0
DTI D0 D10

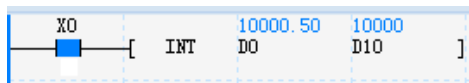
6.5.5 INT

INT (S) (D)										MC200 MC100 MC280					
INT S D										6					
S	REAL								D				V		R
D	INT			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R

S 
D

S 32767 D=32767 S -32768 D=-32768

1 S
2 D



LD X0
INT D0 D10

X0=ON & D0,D1 =10000.5 D10
D10=10000

6.5.6 DINT

DINT (S) (D)										MC200 MC100 MC280					

MC80 MC280

	Z	R	
	Z	R	

0 D10

MC80 MC280

9999

6.5.9 BIN 16 BCD

					MC200	MC100	MC80	MC280
[	BIN	(S)	(D)	]				

6.5.11 GRY 16

										VC200 VC100 M690000						
GRY S D										5						
S	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R	

S
D



LD X0
GRY À Ÿ &

È S

16

D

5.14 DGBIN 32

										MC200 MC100 MC80 MC280				
┌──┐ ┌──┐		DGBIN		(S)	(D)									
		DGBIN		S	D									
S	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD		V		
D	DWORD			KnY	KnM	KnS	KnLM		D			V		

S 1 Ĩ İ X0 J 3435973836 19254 LD X0
D [DGBIN DO] DGBIN 10
X0=ON D0,D1 =0xCCCCCCCC 32
S 32 D10,D11 D10,D11 =0x88888888 2290649224
DD 5 Å & 0 &

5.15 SEG 7

										MC200 MC100 MC80 MC280			
┌──┐ ┌──┐		SEG		(S)	(D)								

6.5.16 ASC ASCII

										MC200	MC100	MC80	MC280
[ASC (S1~S8) (D)]													
ASC S1 S8 D										19			
S1	WORD												
S2	WORD												
S3	WORD												
S4	WORD												
S5	WORD												
S6	WORD												
S7	WORD												
S8	WORD												
D	WORD								D	C	T	V	Z R

S1 S8 8 0
ASCII 0x21 0x7E
8 0X00
D

S1 S8 ASCII
D SM186=OFF
ASCII SM186=ON D
8 1 ASCII 182

MO [ASC 12345678 12849 DO]

LD M0
ASC 12345678 D0
M0=ON ASCII
• SM186=OFF D=0x3231
D1=0x3433 D2=0x3635 D3=0x383
• SM186=ON D0=0x31
D2=0x33 D3=0x34 D4=0x35 D5=0x36 D6=0x37
D7=0x38

6.5.17 ITA 16 16 ASCII

										MC200	MC100	MC80	MC280
[ITA (S1) (D) (S2)]													

										MC200 MC100 MC80 MC280					
— — [ATI (S1) (D S2)]															
ATI S1 D S2										7					
S1		KnX	KnY	KnS	KnLM	KnSM	D		T	V	Z	R			
D			KnY	S	KnLM		D	C	T	V	Z	R			
S2		KnX	KnY	KnS	KnLM	KnSM	D	C	T	V	Z	R			

S1 ASCII

0x30 S1 0x39 0x41 **S1** 0x46 SM186=OFF

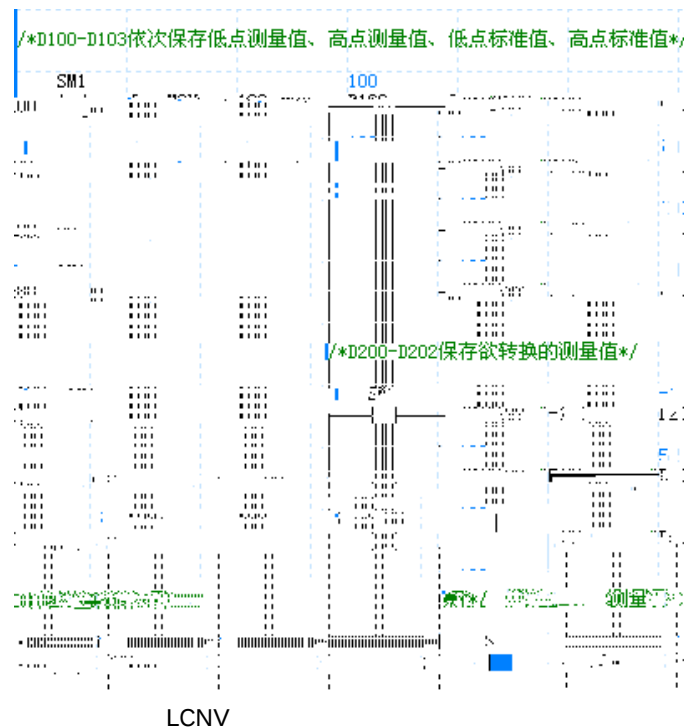
S1 Ü

PLC

$$\begin{array}{ccccccc}
 & V_{ML} & & V_{MH} & & V_{SL} & & V_{SH} \\
 & & & & & S_n & & D_n \\
 A & (V_{SL} - V_{SH}) / (V_{ML} - V_{MH}) * 10000 \\
 B & V_{SL} - (V_{ML} * A / 10000) \\
 D_n & (S_n * A / 10000) - B
 \end{array}$$

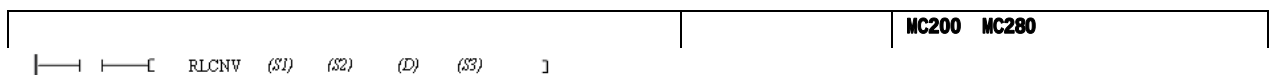
 D_n

32767 32767 -32768 -32768



D300 = -10
D301 = 50
D302 = 150

6.5.20 RLCNV

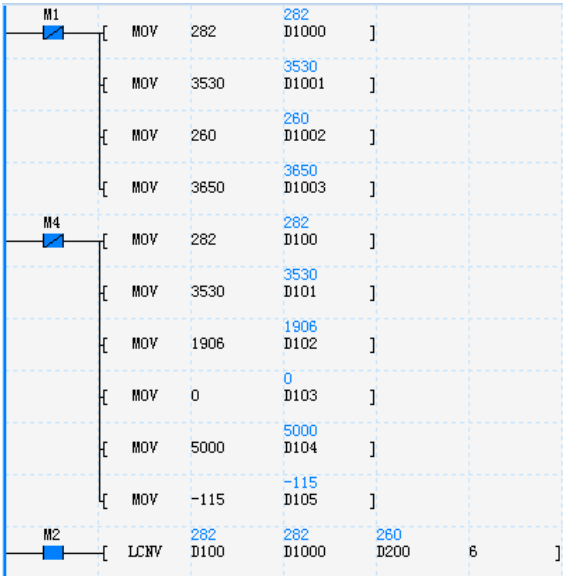


S3 1 S3 64

PLC

$$V_{MH} \qquad V_{SL} \qquad V_{ML} \qquad V_{SH}$$
$$S_n$$
$$D_n$$
$$A \quad (V_{SL} \ V_{SH})/(V_{ML} \ V_{MH}) * 10000$$
$$B \quad V_{SL} \ (V_{ML} * A/10000)$$
$$D_n \ (S_n * A/10000) \ B$$

$$D_n \qquad 32767 \qquad 32767$$
$$-32768 \qquad -32768$$



```
LDI M1
RMOV 282 D1000
RMOV 3530 D1002
RMOV 260 D1004
RMOV 3650 D1006
LDI M4
RMOV 282 D100
RMOV 3530 D102
RMOV 1906 D104
RMOV 0 D106
RMOV 5000 D108
RMOV -115 D110
LD M2
RLCNV D100 D100 D1000 D200 6
M2=ON LCNV
```

D200(D201) = 260
D202(D203) = 3650
D204(D205) = 1955
D206(D207) = -34.3288
D208(D209) = 5184.267
D210(D211) = -154.357

6.6

6.6.1 WAND

</									
--	--	--	--	--	--	--	--	--	--

S11

S22

D



X0=ON

D0=2#101

1

1

LD X0

WAND

D0 D1 D10

S1S2

D

S1

S2

D

1

2

X0

[

WXOR

46739

D0

37678

D1

9661

D10

]

LD

X0

WXOR

D0

D1

D10

X0=ON

D0=2#1011011010010011

46739

D1=2#1001001100101110

37678

D10

D10=2#0010010110111101

9661

S1

S2

D

6.6.4 WINV

[WINV (S) (D)]											MC200 MC100 MC80 MC280					
WINV S D											5					
S	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R	

S

D

X0

[

WINV

46739

D0

18796

D10

]

LD

X0

WINV

D0

D1

D10

X0=ON

D0=

46739

D10=

18796

S

D

6.6.5 DWAND

[DWAND (S1) (S2) (D)]										MC200 MC100 MC80 MC280				
DWAND S1 S1 D										10				
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V	R

6.6.6 DWOR

										MC200 MC100 MC80 MC280					
[DWOR (S1) (S2) (D)]															
DWOR S1 S2 D										10					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R

D**S1** 1**S2** 2**D**

LD X0
 DWOR D0 D2 D10

X0=ON D0, D1 =2#10110010101001101110011001010010 2997282386
 D2, D3 =2#00111010001110110011000100110011 976957747
 D10, D11 D10, D11 =2#1011101010111111111011101110011 3133142899

S1 S2

6.6.7 DWXOR

										MC200 MC100 MC80 MC280					
[DWXOR (S1) (S2) (D)]															
DWXOR S1 S2 D										10					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R

S1 1**S2** 2**D**

LD X0
 DWXOR D0 D2 D10

X0=ON D0,D1 =2#10110010101001101110011001010010 2997282386
 D2,D3 =2#00111010001110110011000100110011 976957747
 D10, D11 D10, D11 =2#10001000100111011101011101100001 2292045665

S1 S2**D**

6.6.8 DWINV

										MC200 MC100 MC80 MC280					
[DWINV (S) (D)]															
DWINV S D										7					
S	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R

S**D**

LD X0
 DWINV D0 D10

X0=ON D0,D1 =2#10110010101001101110011001010010 2997282386
 D10,D11 D10,D11 =2#01001101010110010001100110101101 1297684909

S**D**

6.7

6.7.1 ROR 16

ROR (S1) (D) (S2)										MC200 MC100 MC80 MC280					
										SM181					
ROR S1 D S2										7					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1 1

D

S2 2

S1

S2

D

SM181

0

Kn

Kn

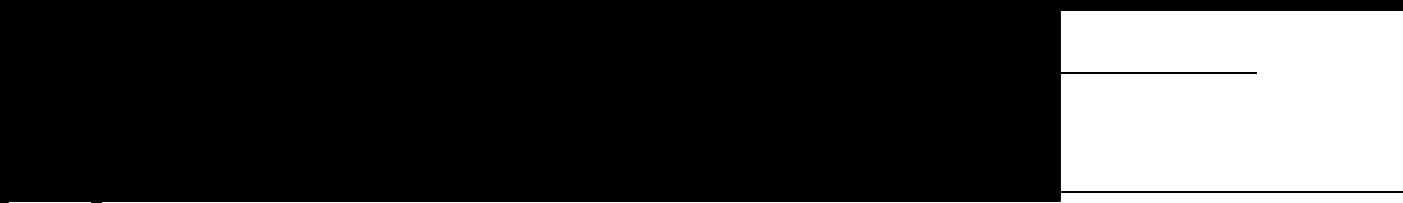
4#p0>2öp0 »8öUD 'ñ Ÿ tme" 6fgyöN«1y?78ká 0U29µ+8p'A€ „ \$?•W ; !PET@[Rµà/p Á

6.7.2 ROL 16

ROL			(S1) (D) (S2)						MC200 MC100 MC80 MC280									
									SM181									
ROL S1			D S2						7									
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R			
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R			
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R			

S1 1
DA 6 q
S2 2

S1
S2 D
é ħp t.¿) > • Dˆ ã



6.7.6 DROL 32

[DROL (S1) (D) (S2)]										MC200 MC100 MC80 MC280					
										SM181					
DROL S1 D S2										9					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1 1 0 Kn Kn 8
D
S2 2

MO [DROL DO D10 30]

LD M0
DROL D0 D10 30

S1 M0=ON D0,D1 =2#10110011100110001001110010101100 3013123244
S2 30 D10,D11 D10,D11
 =2#00101100111001100010011100101011 753280811 SM181=ON
 SM181 ROL

6.7.7 DRCR 32

[DRCR (S1) (D) (S2)]										MC200 MC100 MC80 MC280					
										SM181					
DRCR S1 D S2										9					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1 1 0 Kn Kn 8
D
S2 2

MO [DRCR DO D10 11]

LD M0
DRCR D0 D10 11

S1 1 M0=ON D0,D1 =2#10110011100110001001110010101100 3013123244
 SM181 SM181=OFF 11 D10,D11 D10,D11
S2 =2#00101011000101100111001100010011 722891539 SM181=ON
 2 RCR

6.7.8 DRCL 32

DRCL (S1) (D) (S2)											MC200 MC100 MC80 MC280					
											SM181					
DRCL S1 D S2											9					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	

S110KnKn8

D

S22



LD M0
DRCL D0 D10 25

S1SM181S2

D

1M0=ON D0,D1 =2#10110011100110001001110010101100 3013123244
SM181=OFF 25 D10,D11 D10,D11
=2#00101100010110011100110011001100 1488165020 SM181=ON
2 RCL

6.7.9 SHR 16

 [SHR (S1) (D) (S2)]												MC200 MC100 MC80 MC280					
SHR S1 D S2												7					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		

S11

D

S22



LD M0
SHR D0 D10 5

S1S2

D

5

01111101011011011100

0000001111101101110

M0=ON D0=2#0111101011011100 31452 5 D10
D10=2#0000001111010110 982

6.7.10 SHL 16

SHL (S1) (D) (S2)										MC200 MC100 MC80 MC280					
SHL S1 D S2										7					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

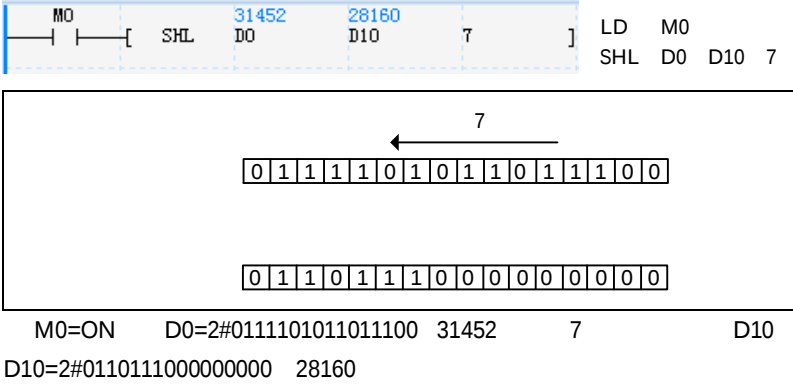
S1 1

D

S2 2

S1
S2 D

S2 0 S1
Kn Kn 4



6.7.11 DSHR 32

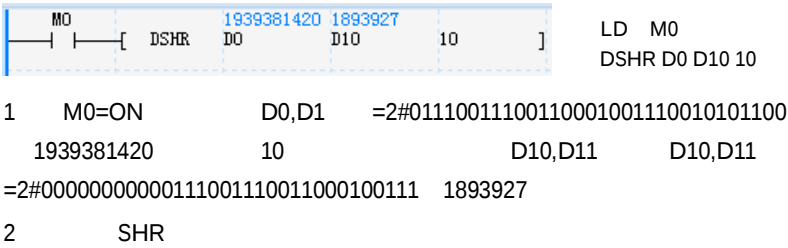
DSHR (S1) (D) (S2)										MC200 MC100 MC80 MC280					
DSHR S1 D S2										9					
S1	DWORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D	DWORD			KnY	KnM	KnS	KnLM		D		C		V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1 1 S2 0 S1 Kn Kn 8

D

S2 2

S1
S2 D



6.7.12 DSHL 32

DSHL (S1) (D) (S2)]		MC200	MC100	MC80	MC280

6.7.14 SFTL

										MC200 MC100 MC80 MC280			
SFTL (S1) (D) (S2) (S3)													
SFTL S1 D S2 S3										9			
S1	BOOL		X	Y	M	S	LM	SM		C	T		
D	BOOL			Y	M	S	LM			C	T		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V Z R
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V Z R

S11

D

S2

S3

1

2

3

LD M0

SFTL X0 M10 10 3

X2

X1

X0

M19

M18

M17

M16

M15

M14

M13

M12

M11

M10

1 M0=ON

M10

10

3

2 X0=1 X1=0 X2=1 M10=0 M11=1 M12=1 M13=0 M14=0

M15=1 M16=0 M17=0 M18=0 M19=1

3 X0 X2 M10=1 M11=0 M12=1 M13=0 M14=1 M15=1

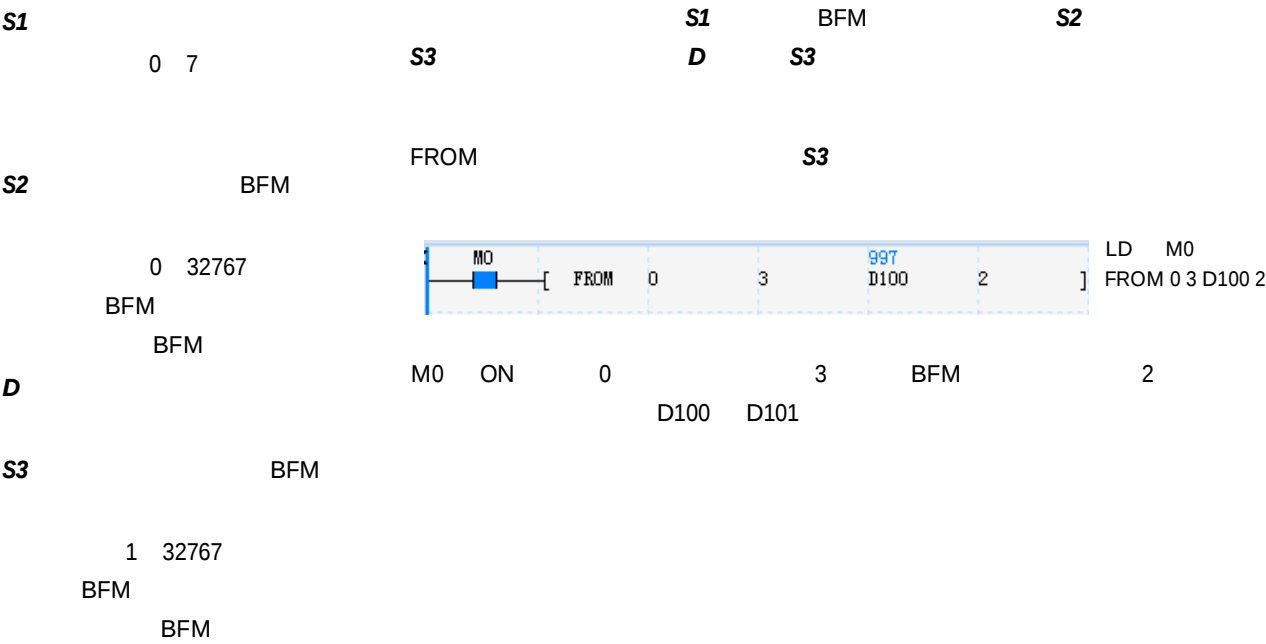
M16=0 M17=0 M18=1 M19=0

MC

6.8

6.8.1 FROM

FROM (S1) (S2) (D) 0										MC200				
FROM S1 S2 D S3										9				
S1	INT													
S2	INT													
D	INT							D				V	R	
S3	INT													



FROM

0 3

LD M0

FROM 0 3 D100 2

M0 ON

0 3

D100 D101

2

FROM

0 3

LD M0

FROM 0 3 D100 2

M0 ON

0 3

D100 D101

2

6.8.2 DFROM

												MC200 MC280					
DFROM S1 S2 D S3												10					
S1	INT																
S2	INT																
D	DINT								D					V		R	
S3	INT																

BFM

S1

0 7

S1

BFM

S2

S3

D

S3

S2

BFM

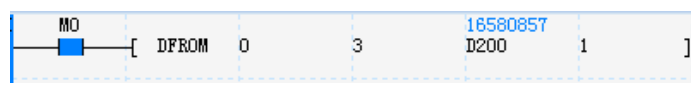
DFROM

S3

0 32767

BFM

BFM



LD M0

DFROM 0 3 D200 1

M0 ON 0 3 BFM 1

S3

BFM

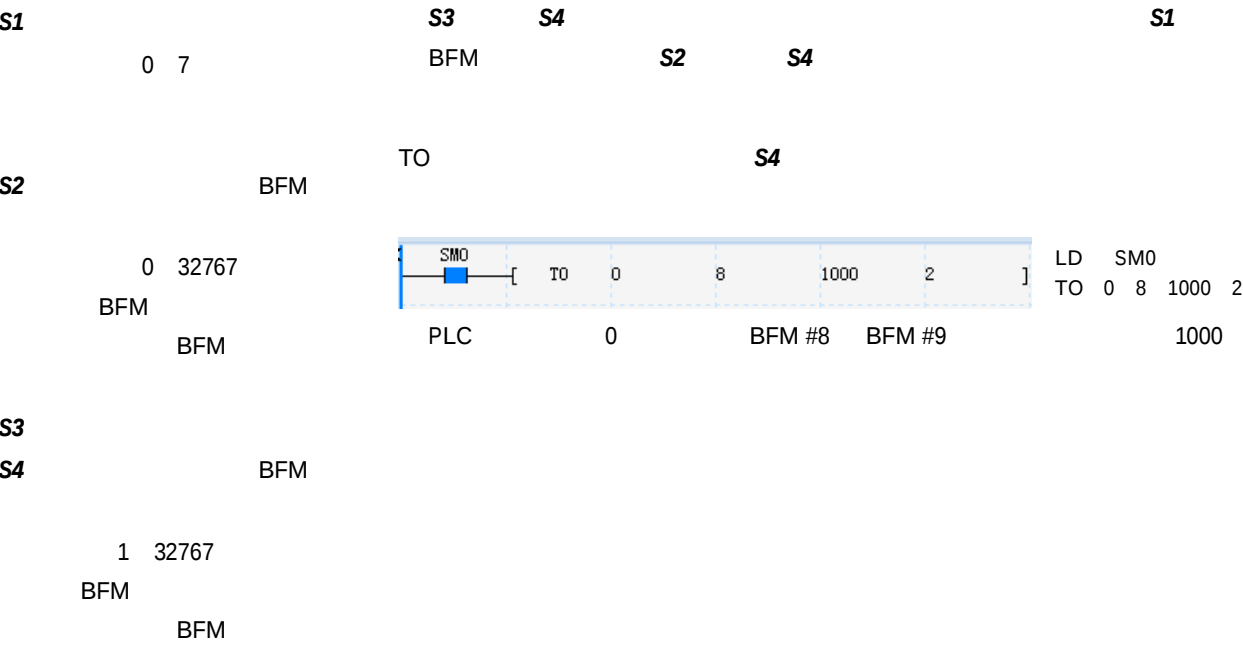
D200,D201

1 32767

BFM

6.8.3 TO

												MC200 MC280					
TO S1 S2 S3 S4												9					
S1	INT																
S2	INT																
S3	INT								D					V		R	
S4	INT																



6.8.4 DTO

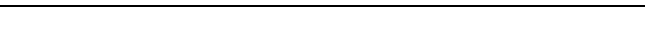
												MC200 MC280					
DTQ S1 S2 S3 S4												10					
S1	INT																
S2	INT																
S3	DINT								D					V		R	
S4	INT																

Diagram illustrating a 32-bit word structure, likely representing a PLC register or memory location. The word is divided into four 8-bit bytes.

The word is labeled with **S1**, **S2**, **S3**, and **S4** at the top, indicating different sections or components.

The word is also labeled with **LD**, **SM0**, and **DT0** at the bottom, indicating different data types or functions.

The word is divided into four 8-bit bytes, each containing a value:

- Byte 1 (S1): 0
- Byte 2 (S2): 32767
- Byte 3 (S3): 8
- Byte 4 (S4): 16711935

The word is also labeled with **BFM** (Bit Field Memory) and **BFM#8** (Bit Field Memory #8) at the bottom, indicating the memory address or range.

6.8.5 VRRD

												MC200 MC100			
VRRD S D												5			
S	WORD														
D	WORD									D				V	

S

0 255

D

0 255

LD M0

VRRD 0 D10

M0 ON 0 D10

6.8.6 REFF

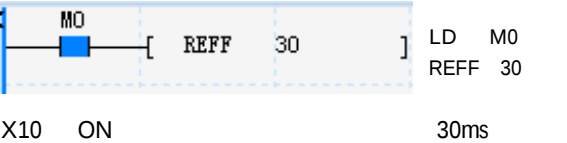
										MC200 MC100 MC80 MC280					
REFF S										3					
S	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S

- MC200

0 64ms 64
- 64
- MC100

0 8 16 32 64
- 8 0 16 8
- 32 16 64 32
- 64



X0 X17

6.8.7 REF I/O

										MC200 MC100 MC80 MC280					
REF D S										5					
D	BOOL		X	Y											
S	INT														

- D

X/Y

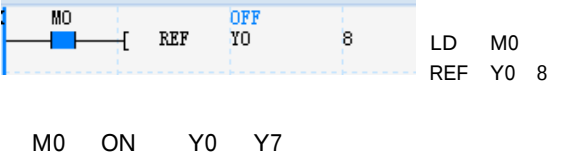
8

X0 X10 X20 ě
- Y0 Y10 Y20 ě
- 0
- S

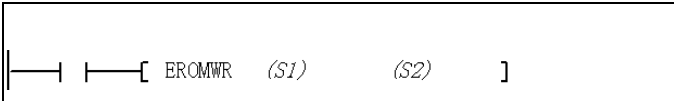
8 16 256 8

- 1 Xn Yn 8
- 2 8
- 3 FOR-NEXT CJ
- REF
- 4
- REF
- 5

PLC



6.8.8 EROMWR EEPROM

										MC200 MC100 MC280					
EROMWR S1 S2										6					
S1	WORD								D						R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

6.8.9 PR

PR											MC200 MC280					
PR (S) (D)											5					
S	WORD								D		C	T		R		
D	BOOL			Y												

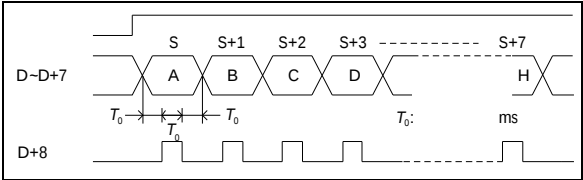
S

D Y

1 S S+7 8 1

2 SM71 SM71

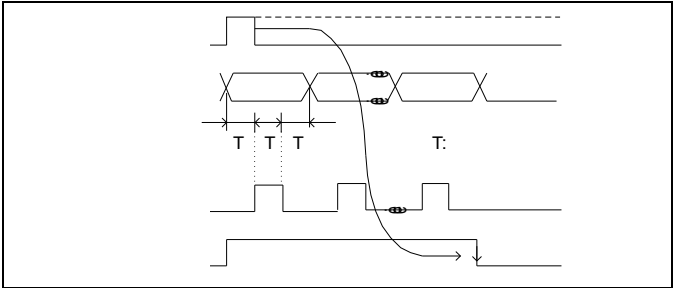
D D+7 Y0



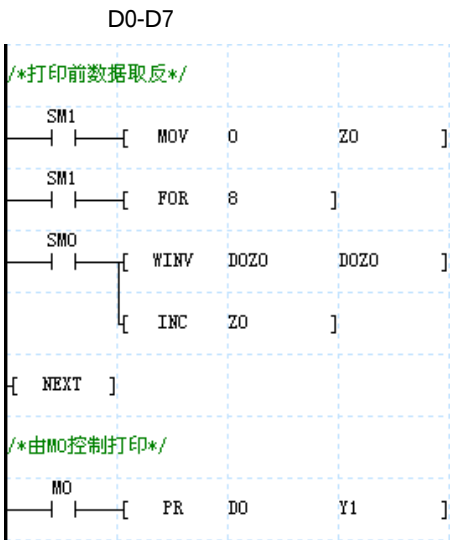
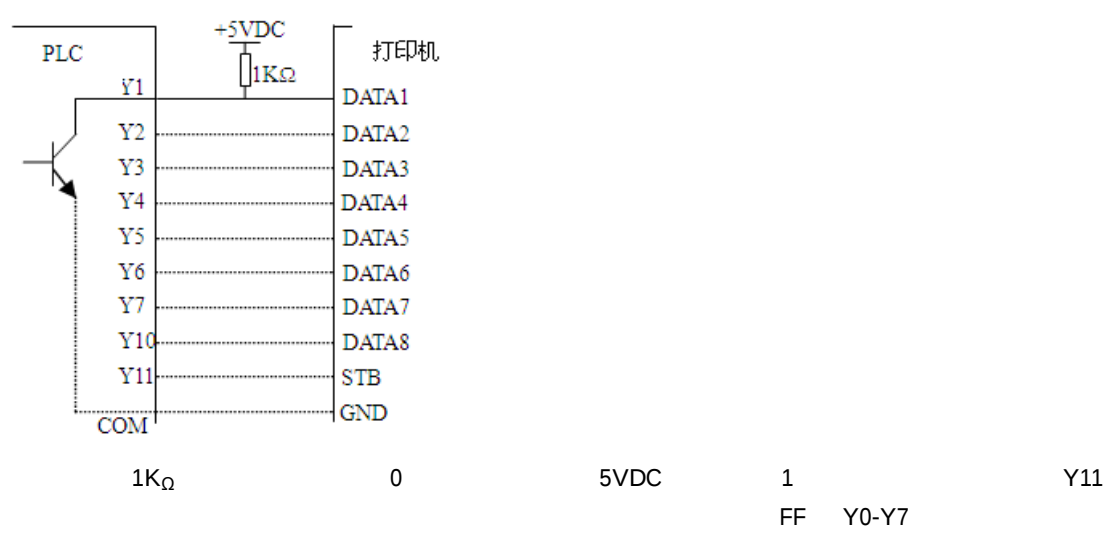
3 SM70 OFF 8

ON 1 16 H00 NUL

SM70 ON



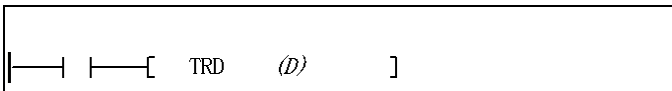
- 1
- 2



- 1
 - 2
 - 3
- SM71

6.9

6.9.1 TRD

										MC200 MC100 MC280						
TRD D										3						
D	WORD								D				V		R	

D

7

D

TRD

M0



[

TRD

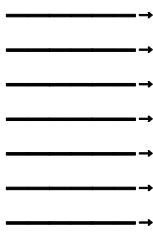
D10

]

LD M0
TRD D10

M0 ON

D10 7

	SD100		2000 2099		D10	
	SD101		1 12		D11	
	SD102		1 31		D12	
	SD103		0 23		D13	
	SD104		0 59		D14	
	SD105		0 59		D15	
	SD106		0 6		D16	

6.9.2 TWR

TWR (S)		MC200 MC100 MC280
TWR S		3

6.9.3 TADD

[TADD (S1) (S2) (D)]												MC200 MC100 MC280					
												SM180			SM181		
TADD S1 S2 D												7					
S1	WORD								D	SD			V		R		
S2	WORD								D	SD			V		R		
D	WORD								D				V		R		

D12	59		D22	58		D32	57
-----	----	--	-----	----	--	-----	----

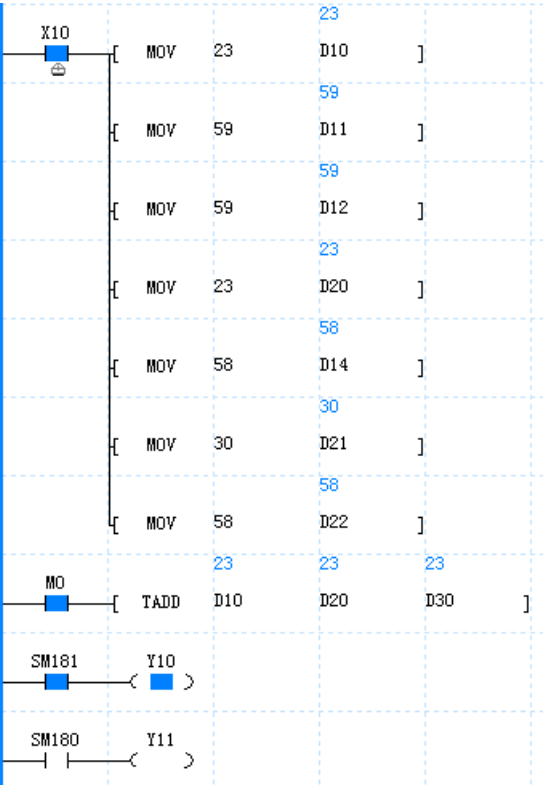
S1 1
S1 3

S2 2
S2 3

D

D 3

SM181 SM180



LD X10
MOV 23 D10
MOV 59 D11
MOV 59 D12
MOV 23 D20
MOV 58 D21
MOV 58 D22
LD M0
TADD D0 D20
D30
LD SM181
OUT Y10
LD SM180
OUT Y11

1 X10 ON D10 3 D20 3
2 M0 ON D10 3 D20 3
0 23 D30 3
0 59 3 SM181 ON SM180 OFF
0 59

S1			S2			D	
D10	23		D20	23		D30	23
D11	59		D21	58		D31	58

6.9.4 TSUB

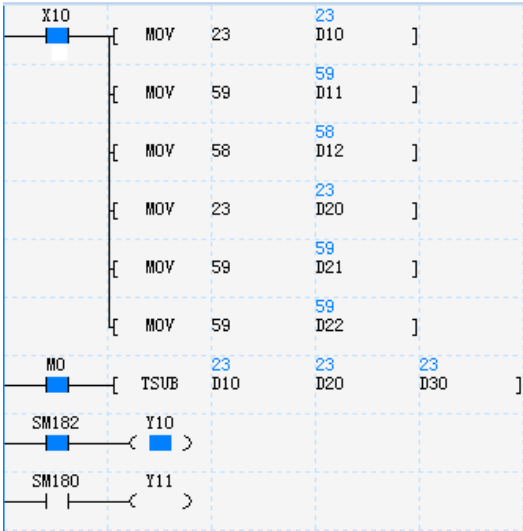
[TSUB (S1) (S2) (D)]												MC200 MC100 MC280					
												SM180				SM182	
TADD S1 S2 D												7					
S1	WORD									D	SD			V		R	
S2	WORD									D	SD			V		R	
D	WORD									D				V		R	

S1 1
S1 3

S1			S2			D	
D10	23		D20	23		D30	23
D11	59		D21	59		D31	59
D12	58		D22	59		D32	59

S2 2
S2 3

D
D 3
SM182 SM180



```
LD X10
MOV 23 D10
MOV 59 D11
MOV 58 D12
MOV 23 D20
MOV 59 D21
MOV 59 D22
LD M0
TSUB D10 D20 D30
LD SM182
OUT Y10
LD SM180
OUT Y11
```

1	X10	ON		D10	3	D20	3
2	M0	ON	D10	3		D20	3
			D30	3			
3			SM182	ON		SM180	OFF

0 23
0 59
0 59

Diagram illustrating the connection between a PLC and a motor (M0) using a relay (D1) and a timer (D2).

PLC Connections:

- Input: **D1** (Digital Input 1) connected to **M0** (Motor).
- Output: **D2** (Digital Output 2) connected to **M0** (Motor).

Motor (M0) Connections:

- Input: **D1** (Digital Input 1) connected to **M0** (Motor).
- Output: **D2** (Digital Output 2) connected to **M0** (Motor).

PLC Ladder Logic:

```

    LD M0
    MOV 1000 D100
    LD M1
    MOV 1000 D200
    LD M10
    OUT Y0
  
```

Motor Ladder Logic:

```

    LD M0
    MOV 1000 D100
    LD M1
    MOV 1000 D200
    LD M10
    OUT Y0
  
```

Motor Parameters:

- Motor: **M0**
- Input: **D1**
- Output: **D2**
- Timer: **D100**
- Timer: **D200**
- Timer: **M10**
- Timer: **Y0**

6.9.6 DCMP = < > <> >= <=

										MC200 MC100 MC280								
[	—	—	DCMP=	(S1)	(S2)	(D)	]					7						
[	—	—	DCMP<	(S1)	(S2)	(D)	]											
[	—	—	DCMP>	(S1)	(S2)	(D)	]											
[	—	—	DCMP<>	(S1)	(S2)	(D)	]											
[	—	—	DCMP>=	(S1)	(S2)	(D)	]											
[	—	—	DCMP<=	(S1)	(S2)	(D)	]											
DCMP								S1	S2	D								
DCMP								S1	S2	D								
DCMP								S1	S2	D								
DCMP								S1	S2	D								
DCMP								S1	S2	D								
DCMP								S1	S2	D								
S1	INT								D	SD			V		R			
S2	INT								D	SD			V		R			
D	BOOL			Y	M	S	LM				C	T						

S1

1

S1

3

3

S2

2

S2

3

3

D

D

ON

OFF

S1 S2

BIN

D

S1 S2

2004 9

31 2003 2 29

SM0

[

MOV

2004

2004

D0

]

[

MOV

10

10

D1

]

[

MOV

25

25

D2

]

[

MOV

2004

2004

D10

]

[

MOV

10

10

D11

]

[

MOV

24

24

D12

]

X0

[

DCMP=

2004

2004

D0

D10

OFF

M0

]

[

DCMP<

2004

2004

D0

D10

OFF

M1

]

[

DCMP>

2004

2004

D0

D10

ON

M2

]

[

DCMP<>

2004

2004

D0

D10

ON

M3

]

[

DCMP>=

2004

2004

D0

D10

ON

M4

]

[

DCMP<=

2004

2004

D0

D10

OFF

M5

]

LD SM0

MOV 2004 D0

MOV 10 D1

MOV 25 D2

MOV 2004 D10

MOV 10 D11

MOV 24 D12

LD X0

DCMP= D0 D10 M0

DCMP< D0 D10 M1

DCMP> D0 D10 M2

DCMP<> D0 D10 M3

DCMP>= D0 D10 M4

6.9.7 TCMP = < > <> >= <=

TCMP= (S1) (S2) (D)] TCMP< (S1) (S2) (D)] TCMP> (S1) (S2) (D)] TCMP<> (S1) (S2) (D)] TCMP>= (S1) (S2) (D)] TCMP<= (S1) (S2) (D)]										MC200 MC100 MC280						
TCMP S1 S2 D TCMP S1 S2 D TCMP S1 S2 D TCMP S1 S2 D TCMP S1 S2 D TCMP S1 S2 D										7						
S1	INT								D	SD			V		R	
S2	INT ,								D	SD			V		R	
D																

6.9.8 HTOS

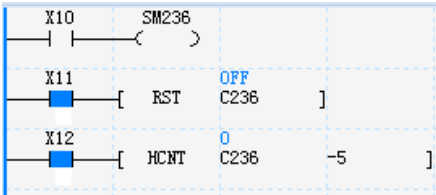
[HTOS (S) (D)]											MC280
HTOS (S) (D)											5
S	WORD	KnX	KnY	KnM	KnS	T	C	D	SD		

6.10 IO

6.10.1 HCNT

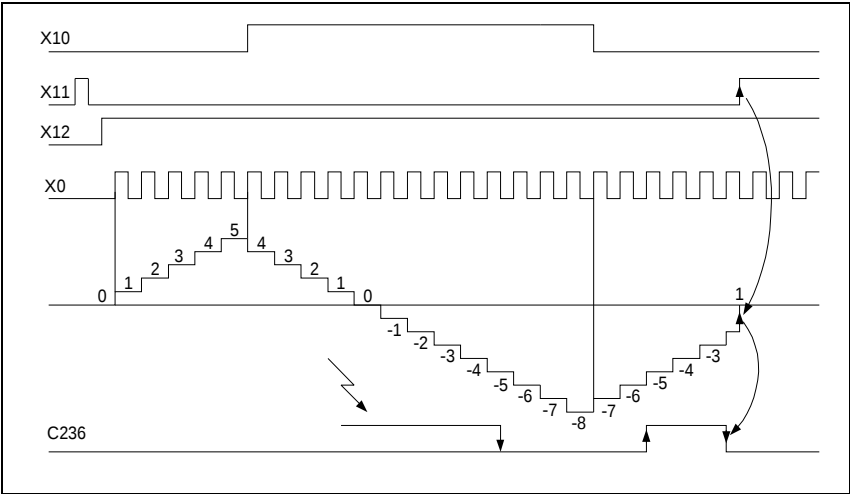
												MC200 MC100 MC80 MC280					
HCNT D S												7					
D	DINT										C						
S	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R		

D
C236 C259
S 32
2147483648 2147483647



LD X10
OUT SM236
LD X11
RST C236
LD X12
HCNT C236 -5

S
HCNT
HCNT SPD
IO
IO



- 1 X12 OFF ON C236 X0 C236
C236 X0 X12 OFF X0 C236
X0
- 2 C236 6 5 C236
C236 5 6 C236
- 3 X11 ON RST C236 C236
- 4

		X0	X1	X2	X3	X4	X5	X6	X7	kHz		
										MC28 0	MC20 0	MC10 0
	C236	/								100	50	
	C237		/									
	C238			/								
	C239				/						10	
	C240					/						
	C241						/					
	C301							/			/	
	C302								/			
	C242	/										
	C243				/						10	
	C244	/										
	C245				/							
	C246									100	50	
	C247										10	
	C303										/	
	C248											
	C249										10	
	C250											
	C251	A	B							50	30	
	C304			A	B							
	C305					A	B				/	
	C306							A	B			
	C252	A	B									
	C253				A	B					5	
	C254	A	B									
	C255				A	B						
	C256 (X10)	A	B									
	C257 (X11)			A	B						/	
	C258 (X12)					A	B					
	C259 (X13)							A	B			
SPD										100	10	
										/	/	
/		0/10	1/11	2/12	3/13	4/14	5/15	6/16	7/17	/	/	

6.10.2 DHSCS

[DHSCS (S1) (S2) (D)]										MC200 MC100 MC80 MC280					
DHSCS S1 S2 D										10					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT										C				
D	BOOL			Y	M	S									

S1

32 DINT
ID x6'S' TM~ ,€
2147483648 2147483647

S2

C236 C259

D

Y M

S

1 DHSCS

HCNT

HCNT

DHSCS

2 DHSCS

Ä

6.10.3 DHSCI

[DHSCI (S1) (S2) (S3)]											MC200 MC100 MC80 MC280					
DHSCI S1 S2 S3											10					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S2	DINT										C					
S3	WORD															

S1

32

DINT

2147483648

2147483647

S2

C236

C259

20

S3

25

HCNT

OFF

ON

DHSCI

S1

S3

DHSCI

S1

S3

4 PLC

DHSP

DHST

DHSCI

DHST

DHSCS

DHSCI

DHSCR

DHSZ

IO

M1

SM236

M0

HCNT

C236

1000

M2

DHSCI

2000

C236

20

C236

Y11

LD

M1

OUT

SM236

LD

M0

DHSCI

2000

C236

20

LD

C236

OUT

Y11

M10

Y20

D0

100

Y12

MOV

0

D0

LD

M10

OUT

Y20

LD>=

D0

100

OUT

Y12

MOV

0

D0

1 DHSCI

HCNT

HCNT

DHSCI

2 DHSCI

DMOV

MOV

DHSCI

3 DHSCI

DHSCS

DHSCR

DHSZ

DHSP

DHST

1 M1 ON C236 X0 OFF ON X0

IO C236 999 1000 C236 1001

1000 C236 C236 Y11 Y11

2 M2 ON DHSCI

C236 2000 20

3 M0 ON SM236 C236 M0 OFF SM236

C236

4 C236 C236 2000 20

M10 ON Y20 Y20

D0 100 Y12 D0

6

6

6.10.4 DHSPI

----- ----- DHSPI (S1) (S2) (S3)										MC280					
DHSPI S1 S2 S3										10					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT									SD					
S3	WORD														

S1 32 DINT
2147483648 2147483647

S2 ,
SD200,SD320,SD340,SD350,SD360,SD370

S3 53,54,55,56,57,58.

DHSP= κ H ♥ SP

6.10.5 DHSCR

DHSCR (S1) (S2) (D)										MC200 MC100 MC80 MC280						
DHSCR S1 S2 D										10						
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S2	DINT										C					
D	BOOL			Y	M	S					C					

2 DHSCR DMOV MOV

DHSCR

S1

32 DINT

2147483648 2147483647

3 DHSCR DHSCI DHSCS DHSZ DHS DHST

6 6

S2

C236 C259

4 PLC DHSCS

D

Y M

S C

C S2

HCNT

OFF ON

DHSCR

S1 D

Y

DHSCR

1 DHSCR

HCNT

HCNT

DHSCR

6.10.6 DHSZ

----- -----[DHSZ (S1) (S2) (S3) (D)										MC200 MC100 MC80 MC280					
DHSZ S1 S2 S3 D										13					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S3	DINT										C				
D	BOOL			Y	M	S									

S1

1 32 DINT
2147483648
2147483647

S2

2 32 DINT
2147483648
2147483647

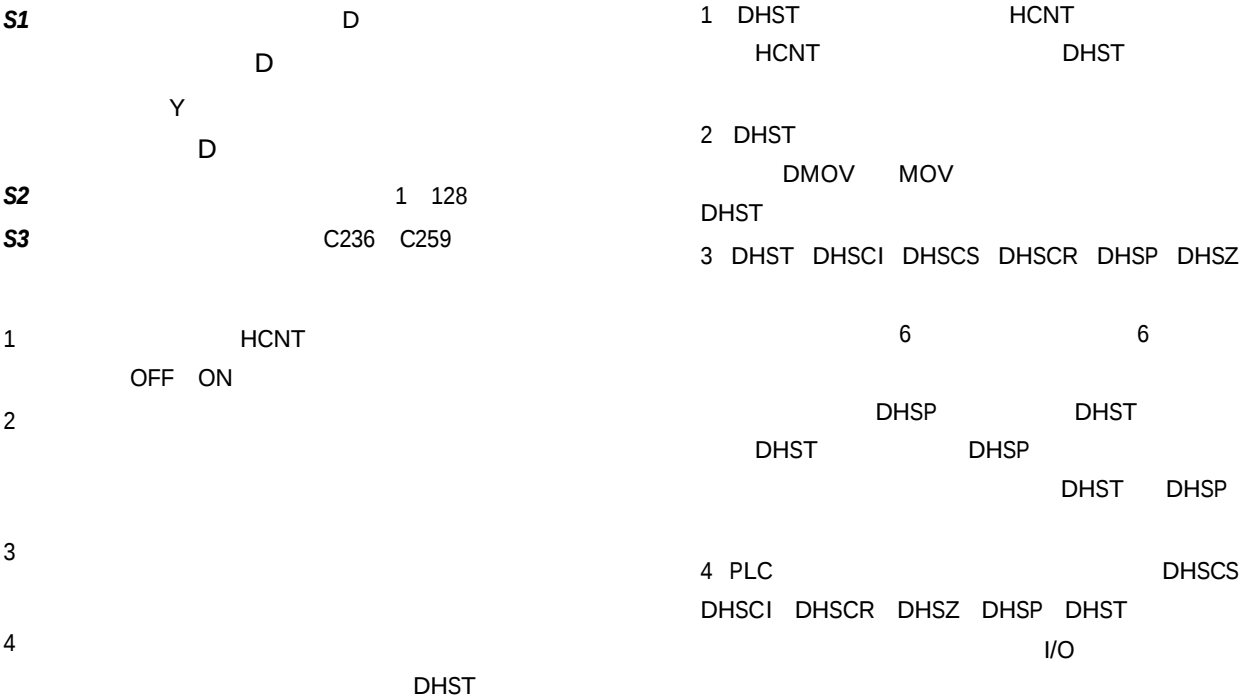
S3

C236 C259

D

6.10.7 DHST

DHST (S1) (S2) (S3)										MC200 MC100 MC80 MC280					
DHST S1 S2 S3										10					
S1	DINT								D						R
S2	INT														
S3	DINT										C				



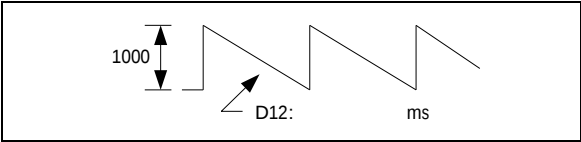
6.10.8 DHSP

[DHSP (S1) (S2) (S3)]										MC200 MC100 MC80 MC280			
DHSP S1 S2 S3										10			
S1	DINT								D				R
S2	INT												

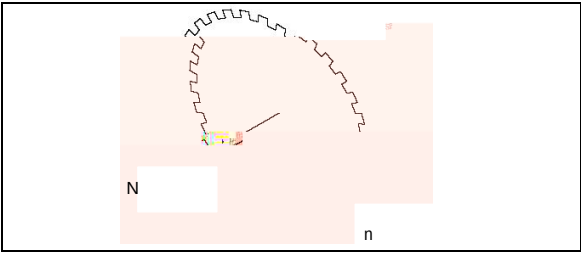
6.10.9 SPD

[SPD (S1) (S2) (D)]												MC200 MC100 MC80 MC280					
SPD S1 S2 D												7					
S1	BOOL		X														
S2	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
D	WORD								D				V		R		

S1 X0 X5
S2 ms S2>0
D 65535



X0 X5 ms

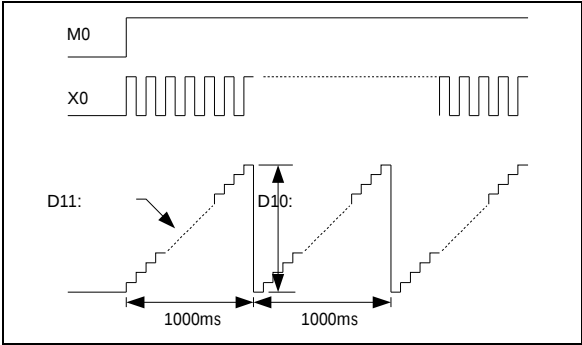


- 1 SPD HCNT 6.10 IO
2 SPD X0 X5
3 SPD 10kHz 10kHz
4 SPD

- 1 M0 ON X0 1000ms D10 D11
1000ms D12 1000ms
2 D10
3 X0 OFF ON 1000ms
D10

SMD	PLSY	10000	0	ON	Y0
M0	SPD	ON	X0	1000	10000

LD SMD
PLSY 10000 0 Y0
LD M0
SPD X0 1000 D10



6.10.10 PLSY

6 PLSY PWM PLSR

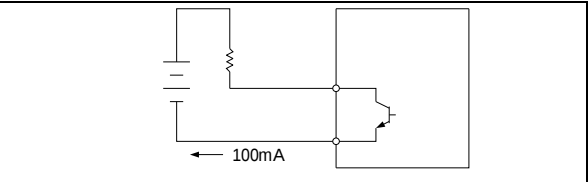
[PLSY (S1) (S2) (D)]										7 PWM PLSY PLSR MC200 MC100 MC80 MC280					
PLSY S1 S2 D										9					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	8 D	SD	C	DHSCS	DHSCR	DHSZ	DHSP
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	DHST	HCNT	C	PLSY	V		R
D	BOOL			Y											

S1 Hz
MC100 MC200 1 100000 Hz MC280
1 200000 Hz S1 0 100000
S2
0 2147483647
S2 0
S2
D MC100 MC200, Y0
Y1 MC280, Y0 Y1 Y2 Y3 Y4
Y5 Y6 Y7

PLC

1 PLC
2 PLC PLC

3 PLSY PWM PLSR



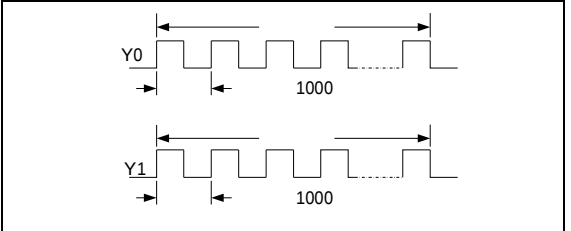
4 OFF PWM PLSY
PLSR

100mA

5

M1	[PLSY 1000 10000 OFF Y1]
	[PLSY 1000 10000 OFF Y0]

LD M1
PLSY 1000 10000 Y1
PLSR 1000 10000 Y0



1 M1 ON Y0 Y1 10000
1000Hz 10000
M0 OFF ON
M0 OFF OFF
2 50 ON 50 OFF

Y Y0
PORT0 Y1 PORT1

3 SM80 Y0 SM81 Y1
1

4 SM82 SM83 Y0 Y1
M0 OFF

5 SD50 Y0 PLSY PLSR

SD51 Y0 PLSY PLSR
SD52 Y1 PLSY PLSR
SD53 Y1 PLSY PLSR
SD54 Y0 Y1 PLSY

PLSR
SD55 Y0 Y1 PLSY PLSR

6 SD50 SD55 DMOV SD5

MOV SD5

7 PLSY

DHSP

6.10.11 PLSR

PLSR(S1)(S2)(S3)(D)											MC200MC100MC80MC280					
PLSRS1S2S3D											10					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S3	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D1	BOOL			Y												



S1 Hz 10 20000 Hz

20000 20000

10 10

MC100 50ms

10

S1/10

S2 PLS 110

2147483647

D MC100 MC200,

Y0 Y1 MC280, Y0 Y1 Y2 Y3

Y4 Y5 Y6 Y7

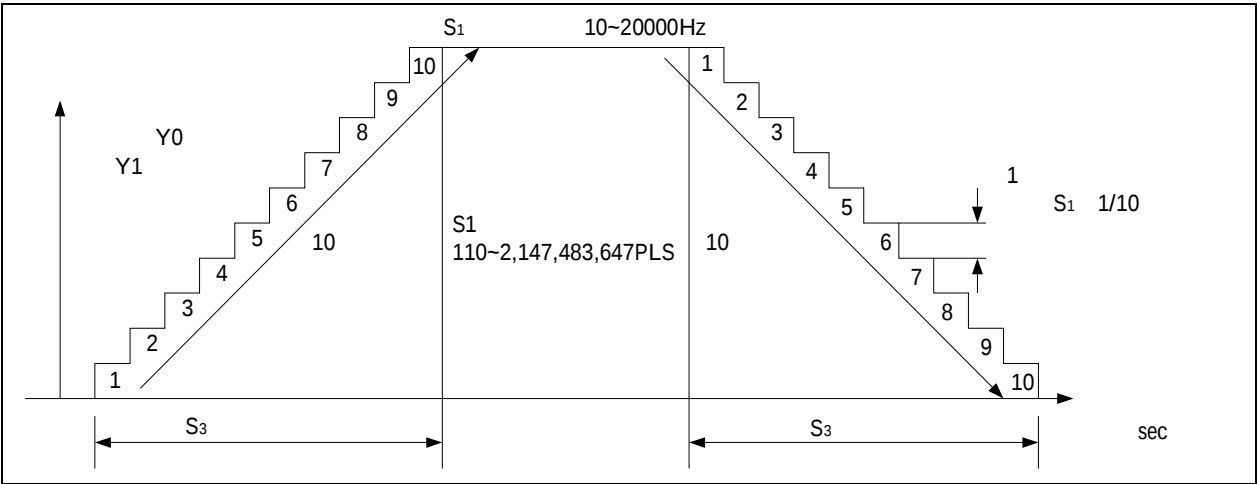
S3 ms

S1 S3<100000 S3=100000/S1

PLSR

S1 S3>S2 909 S3=S2 909/S1

PLSR



1 10 20000Hz

2 PLC

Y0 PORT0

Y1 PORT1

3

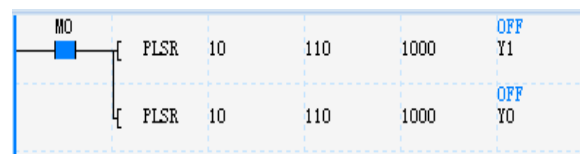
4 2 PLSR

PWM PLSY

5 PWM PLSY PLSR

6 DHSCS DHSCR DHSZ DHSP

DHST HCNT PLSR



LD M0

PLSR 10 110 1000 Y1

PLSR 10 110 1000 Y0

1 M0 ON Y0 Y1

110 M0 OFF

ON M0 OFF

OFF

2

M0 ON OFF

ON

3 SM80 Y0 SM81 Y1

SM80 SM81 1

4 SM82 SM83 Y0 Y1

M0 OFF SM82 SM83 OFF

SM82 SM83 ON

5 SD50 SD55

1 SD50 Y0 PLSY PLSR

2 SD51 Y0 PLSY PLSR

3 SD52 Y1 PLSY PLSR

4 SD53 Y1 PLSY PLSR

5 SD54 Y0 Y1 PLSY PLSR

6 SD55 Y0 Y1 PLSY PLSR

6 SD50 SD55 DMOV SD5

MOV SD5

6.10.12 PLS

									MC200 MC100 MC280						
PLS S1 S2 D1									7						
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D1	BOOL			Y											

S1 D
S2 0 255
D MC100 MC200,
Y0 Y1 MC280, Y0 Y1 Y2 Y3
Y4 Y5 Y6 Y7

1 PLS

2 0
3 SM80 SM81

4 PLS_SET n

D M
LD SM0
DMOV 1 Dn
DMOV 1 Dn 2
DMOV 2 Dn 4
DMOV 2 Dn 6
DMOV 3 Dn 8
DMOV 3 Dn 10

DMOV M Dn 4M 4
DMOV M Dn 4M 2
DMOV Dn 4M
MOV Dn 4M 2
MOV Dn 4M 3
MOV Dn 4M 4

1 PTO PLS
PLS

2 P F_N N
 F_{max} F_{min} T_{up}
 T_{down}
1 N N 1
N :
 $P \frac{(F_N - F_{N-1}) (F_N - F_{N-1}) T_{up}}{2000 (F_{max} - F_{min})}$
2 N N 1
N :
 $P \frac{(F_N - F_{N-1}) (F_N - F_{N-1}) T_{down}}{2000 (F_{max} - F_{min})}$
3
1 N=1 N 1 F_{min}
2 1 1
 $P \frac{(F_1 - F_{min}) (F_1 - F_{min}) (T_{up} - T_{down})}{2000 (F_{max} - F_{min})}$
3
 $P \frac{(F_M - F_{M-1}) (F_M - F_{M-1}) (T_{up} - T_{down})}{2000 (F_{max} - F_{min})}$
4
5 999 999
4 PLC
5
6 PLSY,PLSR,PLS

6.10.13 PLSB

										MC100 MC280						
PLSB (S1) (S2) (S3) (S4) (D)										12						
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S3	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S4	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D1	BOOL			Y												

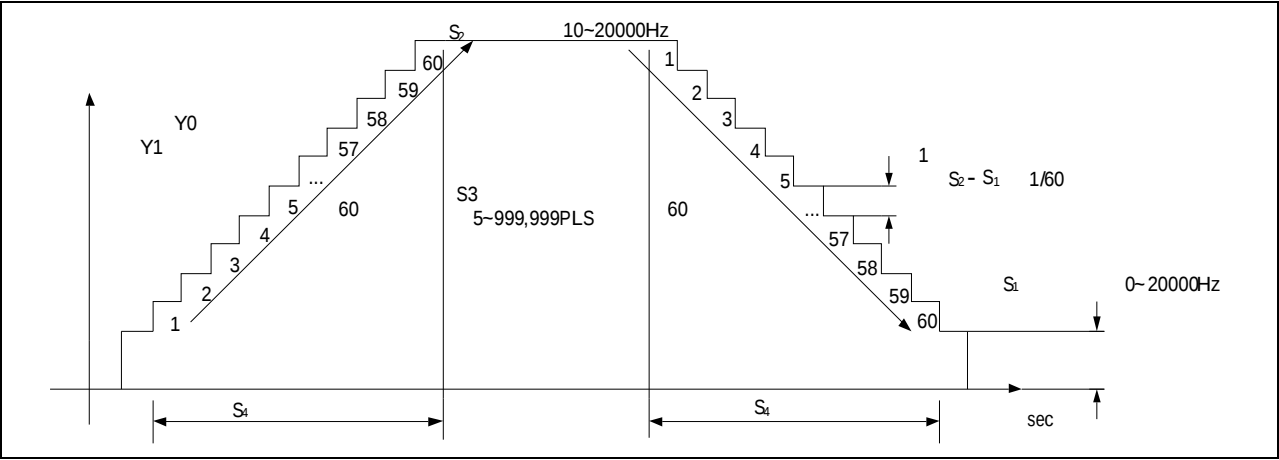
S1 HZ
0 20000Hz

S4 (mS)
0-10000

S2 HZ
10 20000 (Hz)

D
MC100 MC200, Y0 Y1 MC280,
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

S3 (PLS)
5-999999



1 10-20000Hz

M0	[	PLSB	100	10000	10000	1000	OFF	Y1	]
	[	PLSB	100	10000	10000	1000	OFF	Y0	]

2 LD M0
PLSR 100 10000 10000 1000 Y1
PLSR 100 10000 10000 1000 Y0
1 M0 ON Y0 Y1
10000 M0 OFF
ON M0 OFF
OFF
2
M0 ON OFF ON

3 60

5 ()

3 SM80 Y0 SM81 Y1
SM80 SM81 1

6 2 PLSB Y000 Y001
PWM PLSY

4 SM82 SM83 Y0 Y1
M0 OFF SM82 SM83 OFF
SM82 SM83 ON

7 PWM PLSY PLSB

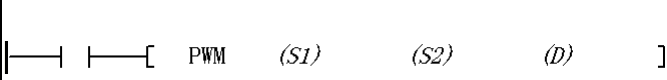
5 SD50 SD55
1 SD50 Y0 PLSB
2 SD51 Y0 PLSB
3 SD52 Y1 PLSB
4 SD53 Y1 PLSB
5 SD54 Y0 Y1 PLSB

8 DHSCS DHSCR DHSZ DHSP
DHST HCNT PLSB

9 Y0 Y1

6 SD55 Y0 Y1 PLSB
6 SD50 SD55 DMOV SD5
MOV SD5

6.10.14 PWM

										MC200 MC100 MC80 MC280						
PWM S1 S2 D										7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	BOOL			Y												

S1 ms/ s
0 32767 ms **S1** 32767

S1
SM84 0 **S1** ms SM84 1 **S1**
s

S2 ms
1 32767

S2
SM84 0 **S1** ms SM84 1 **S1**
s

S2 **S1**

D MC100 MC200, Y0
Y1 MC280, Y4 Y5 Y6 Y7

D **S1** **S2** PWM

1 **S1** 0 OFF **S1=S2**
ON { & Ð M

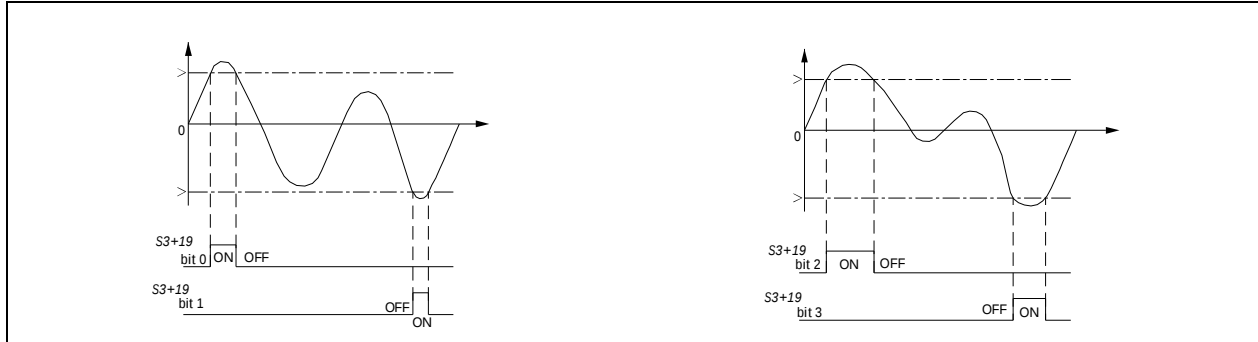
6.11

6.11.1 PID

PID (S1) (S2) (S3) (D)												MC200 MC100 MC80 MC280				
PID S1 S2 S3 D												9				
S1	INT								D					R		
S2	INT								D					R		
S3	INT								D					R		
D	INT								D	R						

8

S3 1 BIT1=ON BIT2=ON BIT5=OFF PID
PID S3 19
PID



9 PID

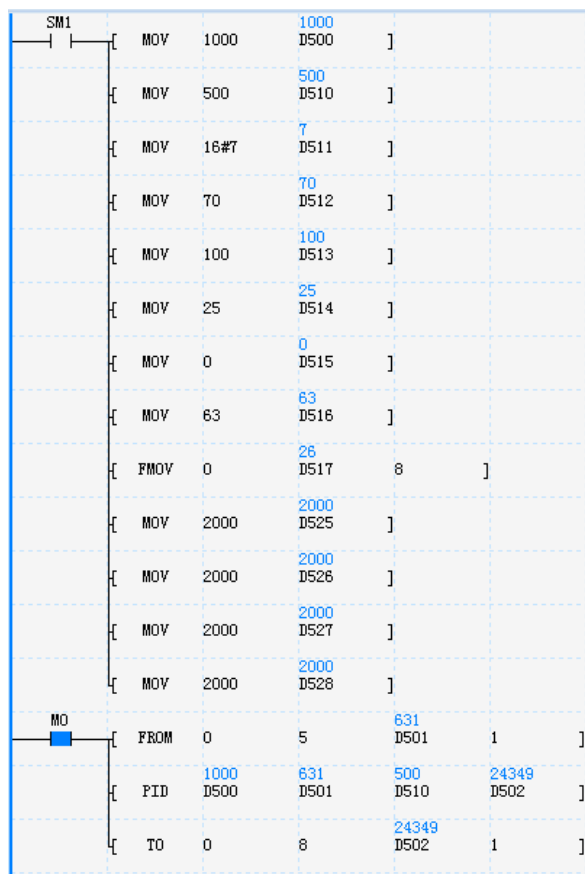
	PID
	$\Delta MV = KP \left\{ (EV_n - EV_{n-1}) + \frac{T_s}{T_i} EV_n + D_n \right\}$ $EV_n = PV_{nf1} - SV$ $D_n = \frac{T_D}{T_s} \frac{\dot{U}_D}{\dot{U}_D} PV_{nf1} - PV_{nf2} - 2PV_{nf1} + \frac{\dot{U}_D}{T_s} \frac{T_D}{\dot{U}_D} D_{n-1}$ $MV_n = \mu MV$
	$\Delta MV = KP \left\{ (EV_n - EV_{n-1}) + \frac{T_s}{T_i} EV_n + D_n \right\}$ $EV_n = SV - PV_{nf1}$ $D_n = \frac{T_D}{T_s} \frac{\dot{U}_D}{\dot{U}_D} 2PV_{nf1} - PV_{nf1} - PV_{nf2} + \frac{\dot{U}_D}{T_s} \frac{T_D}{\dot{U}_D} D_{n-1}$ $MV_n = \mu MV$

EV _n		D _n	
EV _{n-1}	1	D _{n-1}	1
SV		KP	
PV _{nf}		T _s	
PV _{nf1}	1	T _i	
PV _{nf2}	2	T _D	
μMV		U _D	
MV			

// PID

```
LD      SM1          //
MOV     1000         D500 //
MOV     500          D510 //      Ts      1 32767 ms
//
MOV     7            D511 //
MOV     70           D512 //      0 99[ ] 0
MOV     100          D513 //      Kp      1 32767[ ]
MOV     25           D514 //      TI      0 32767 100ms 0
//
```

MOV	0		D515	//	KD	0	100[]	0	
MOV	63		D516	//	TD	0	32767	10ms	0
				//					
FMOV	0		D517	8 //	PID				
MOV	2000		D525	//				0 32767	
MOV	2000		D526	//				0 32767	
MOV	2000		D527	//				0 32767	
MOV	2000		D528	//				0 32767	
//PID									
LD	M0			//	PID				
FROM	0	5	D501	1 //					
PID	D500	D501	D510	D502	//PID	PID S1	S2	S3	D
TO	0	8	D502	1 //	PID				
				//	PID				



Line	Address	Instruction	Comment
1	0	LD SM0	MOV 0 D****
2	PID	S3	20
3	TS	1	1ms
	1	TS	PID
		PID	
4	PID		
		PID	
5		S3 15 S3	
	18		
	PID		
6	S3 1	BIT2 BIT5 ON	
		BIT2 BIT5 OFF	
7	PID	S3 S3 6	
		PID	
8		1	
		PID	
9	PID		
		PID	
		PID	

X2=ON

A/D

D/A

PID

6.11.2 RAMP

[RAMP (S1) (S2) (D1) (S3) (D2)]										MC200 MC100 MC80 MC280						
RAMP S1 S2 D1 S3 D2										12						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D1	INT								D				V		R	
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D2	BOOL			Y	M	S	LM				C	T				

S1

S2

D1

S3 0

D2 0

1

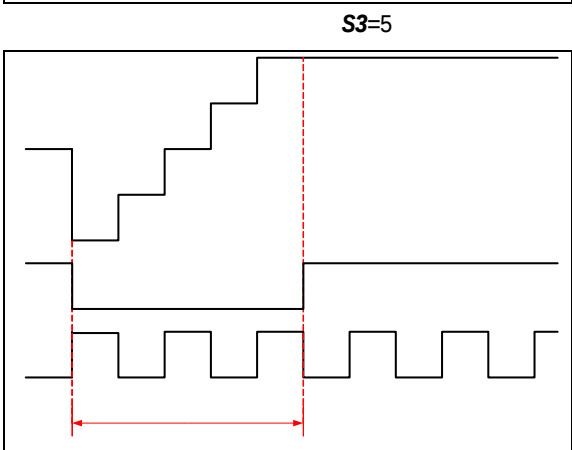
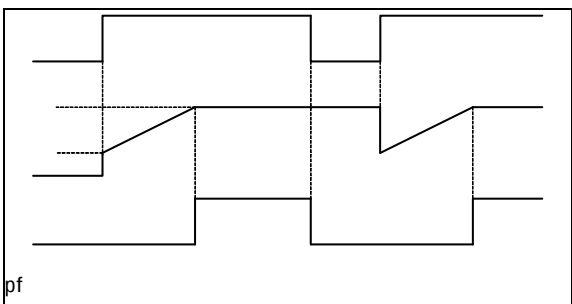
2

3 S1=S2 D1=S2 D2=ON

4 RAMP HACKLE TRIANGLE

100

5. RAMP HACKLE TRIANGLE



```
//
LD SM1
MOV 0 D0
MOV 2000 D1
//X0=ON
LD X0
RAMP D0 D1 D10 1000 M0
//X1=ON
LD X1
TO 0 6 D10 1
```

SM1	[	MOV	0	D0	]
	[	MOV	2000	D1	]
X0	[	RAMP	D0	D1	D10 1000 ON M0
X1	[	TO	0	6	D10 1

1 X0=ON

D10

D10=D0=0

2 2000/1000

D10=D1=2000

D10

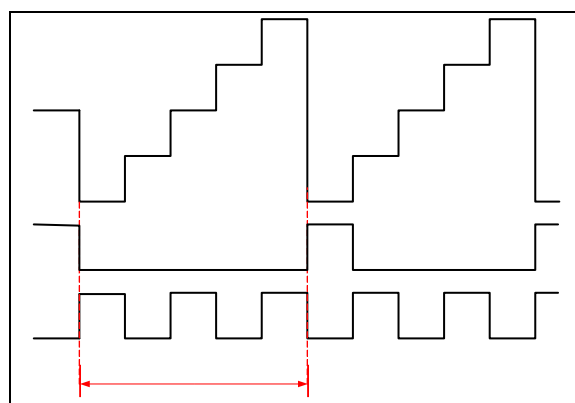
M0=ON

D2 OFF

D1

D10=D0

2

[illegible]

```
LD      X1
TO      0 1 D10 1
```

[illegible]

1 X0=ON D10
D10=D0=0 2 2000/1000 D10=D1=2000
M0=ON X0 ON
D10=D0=0 M0=OFF

OFF **D1**

 D1 **S1**

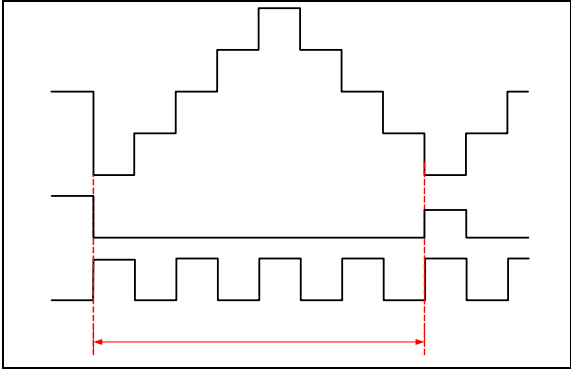
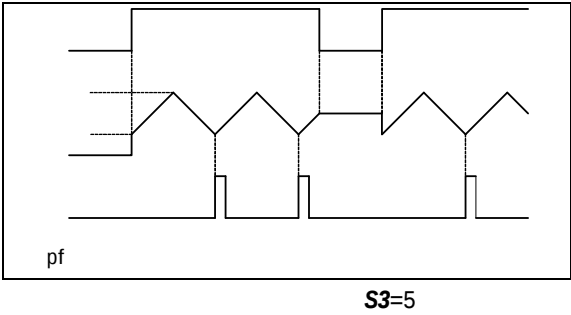
2

6.11.4 TRIANGLE

[TRIANGLE (S1) (S2) (D1) (S3) (D2)]										MC200 MC100 MC80 MC280							
TRIANGLE S1 S2 D1 S3 D2										12							
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
D1	INT								D				V		R		
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
D2	BOOL			Y	M	S	LM				C	T					

S1 1
S2 2
D1 3 S1=S2 D1=S2 D2=ON
S3 S3 0 4 = S3 1 2
D2 5 RAMP HACKLE TRIANGLE
100

D1 S2
D1 S1
D2 ON
ON D2 OFF
D2 OFF D1
D1 S1
D1 S1
//
LD SM1
MOV 0 D0
MOV 2000 D1
//X0=ON
LD X0
TRIANGLE D0 D1 D10 1000 M0
//X1=ON DA



SM1	[	MOV	0	0	D0	]
	[	MOV	2000	2000	D1	]
X0	[	TRIANGLE	D0	2000	D1	1364
X1	[	TO	0	1	D10	1364

1 X0=ON D10
D10=D0=0 2 2000/1000 D10=D1=2000
D10 2
D10=D0=0 M0=ON
X0 ON M0=OFF

D2 OFF D1
D1 S1

2

6.11.5 ABSD

ABSD										MC200 MC280					
ABSD (S1) (S2) (D) (S3)										9					
S1	INT		KnX	KnY	KnM	KnS			D		C	T		R	
S2	INT										C				
D	BOOL			Y	M	S									
S3	WORD														

S1

n 4

S2

D

S3

1 S3 64

1 S1 n (n 2)

S2 n D ON/OFF

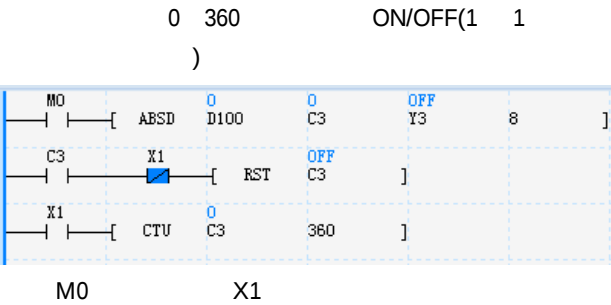
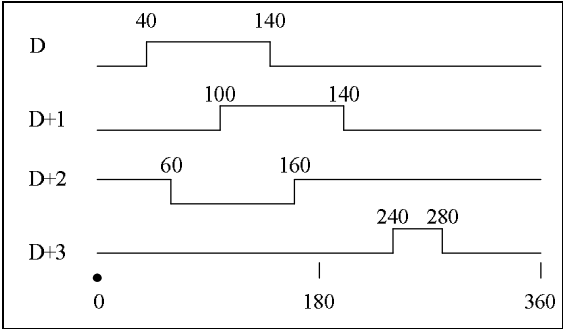
2 / S1 S1 n 2

3 S1 S1 2n 1

S1	40	S1+1	140	D
S1+2	100	S1+3	200	D+1
S1+4	160	S1+5	60	D+2
S1+6	240	S1+7	280	D+3
ë	ë	ë	ë	ë
S1+2n	ë	S1+2n+1	ë	D+n-1

4 ON D n

D+1 140 200



1 S1 k 4

2 S2 S2 C0 C199

3

6 DABSD

	MC200	MC28

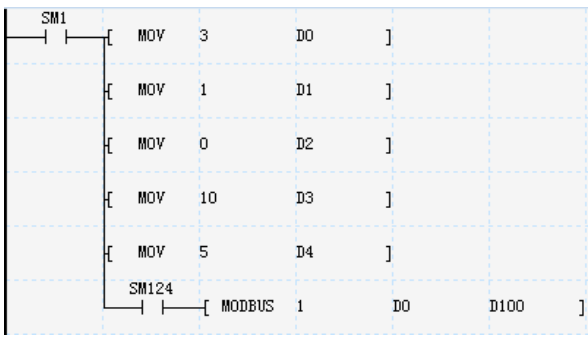
1



6.11.7 ALT

		MC200 MC280
ALT D		11

4



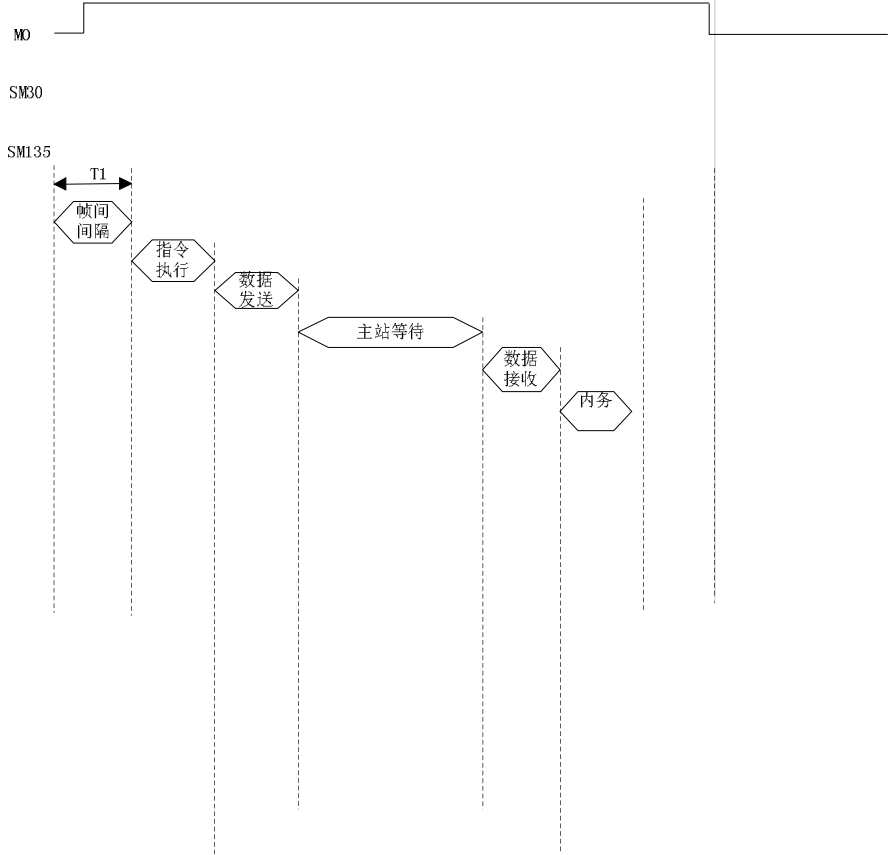
```
LD SM1
MOV 3 D0
MOV 1 D1
MOV 0 D2
MOV 10 D3
MOV 5 D4
AND SM124
Modbus 1 D0 D100
1 Modbus D0
2 D100
3 Modbus CRC
SM136
SD139
4 SM114 SM124
MODBUS MODBUS
Modbus
```

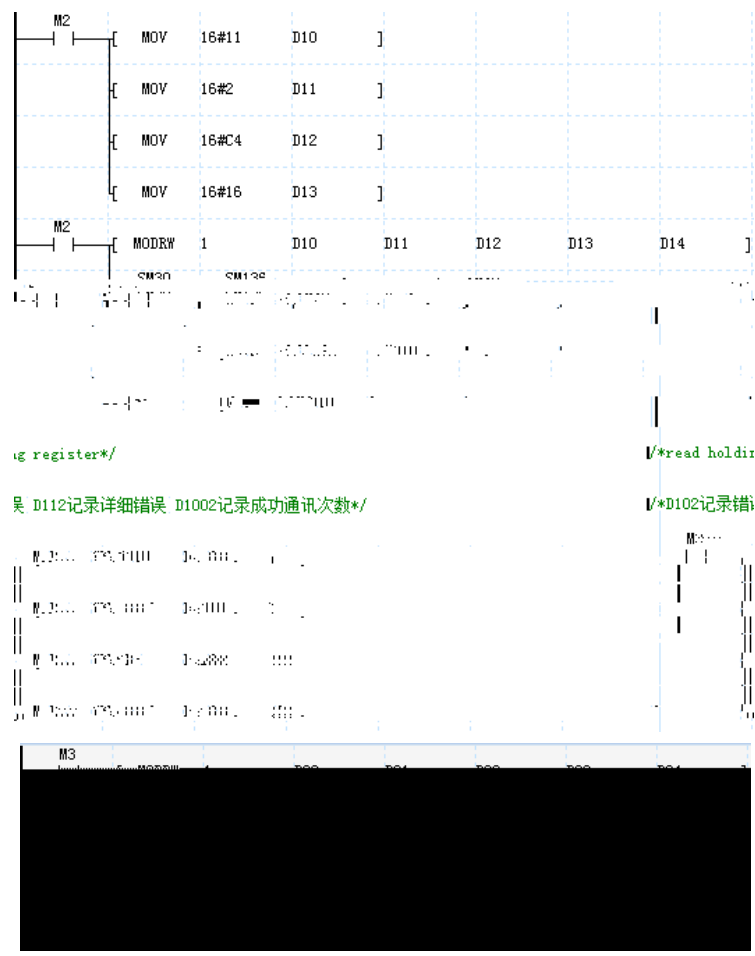
0x01	
0x02	
0x03	
0x10	
0x11	
0x12	/
0x13	

6.12.2 MODRW MODBUS

|—| —|

X0	[	SET	MO	]					
MO	[	MODRW	1	10	1	D2	D3	D4	]
	[	RST	MO	]					





SM30 MODRW MODRW SM136 SD139
MODRW SM30 MODRW SD194 SM136 SD139 SD194
SM30 2 MODRW
SM30 SM135 MODRW
MODRW SM30 MODRW
MODRW
SM30 MODRW
SM30

2

MC100

MV600

MC100

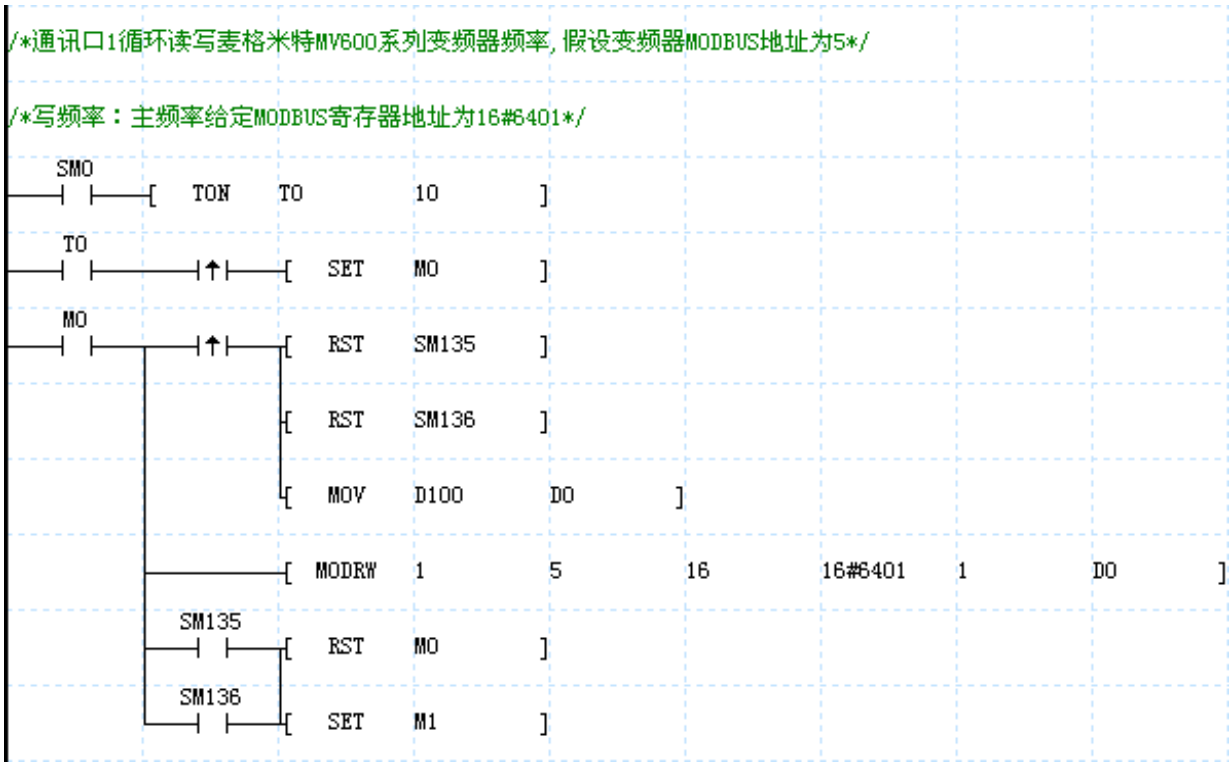
T0

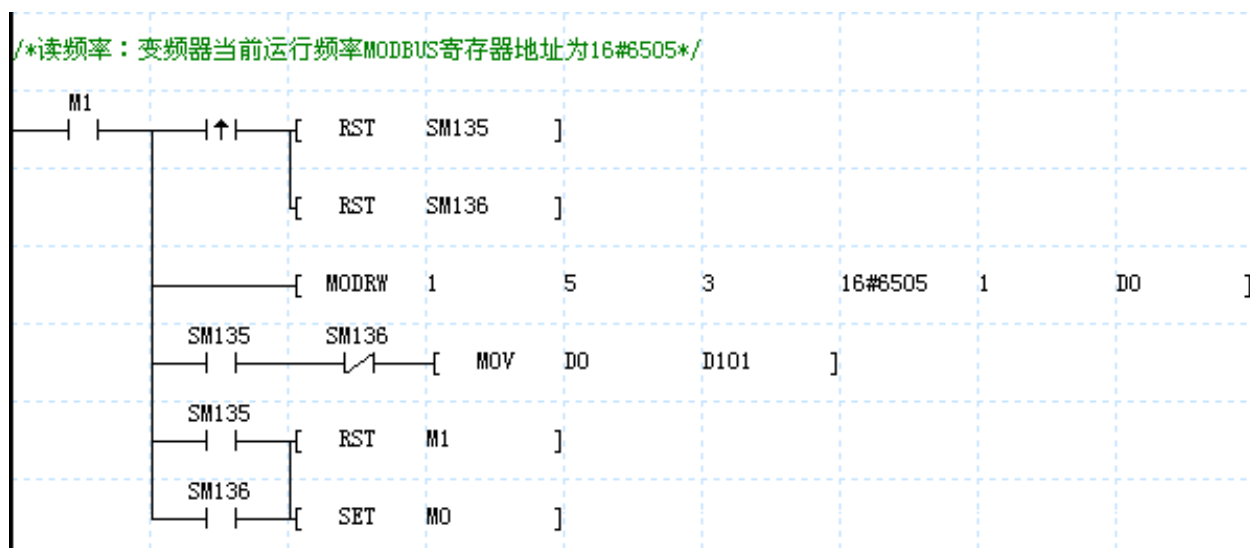
MV600

T0

SM135

SM136





6.12.3 Modlink MODBUS

M90 [MODLINK 1 D200 D46 M114 M156]										MC100 3.000 MC200 3.003					
Modlink S1 S2 S3 S4 S5										12					
S1	INT														
S2	INT	D													
S3	INT	D													
S4	BOOL			M	S					C	T				
S5	BOOL			M	S					C	T				

1

È

MODLINK MODBUS

È MODLINK MODLINK

MODLINK MODLINK

MODLINK MODBUS

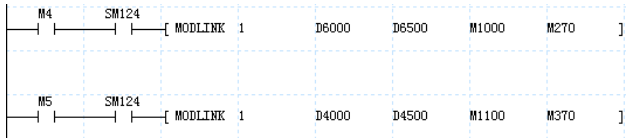
MODLINK





D6000

S2		
S2+1	M	0
S2+2		
S2+3		
S2+4		
S2+5		
S2+6		1
S2+7		
S2+8		
S2+9		
S2+10		
S2+11		
S2+12		
S2+13		
S2+14		
ë		
ë		



SM124

			D
01		1~2000	S5 15 /16
02		1 2000	S5 15 /16
03		1~125	S5
04		1~125	S5
05		0(fixed)	1
06		0(fixed)	1
15		1~1968	S5 15 /16
16		1~123	S5

MODLINK

MODBUS

0 N

S3

S3	0
S3+1	1
S3+2	2
ë	
ë	
S3+N	N

S3

Modbus

0x01	
0x02	
0x03	
0x10	
0x11	
0x12	/
0x13	

S4	0
S4+1	1
S4+2	2
ë	
ë	
S4+N	N

6.12.4 XMT

— —[XMT (S1) (S2) (S3)]										MC200 MC100 MC80 MC280			
XMT S1 S2 S3										7			
S1	INT												
S2	WORD												

6.12.5 RCV

RCV (S1) (D) (S2)										MC200 MC100 MC80 MC280					
RCV S1 D S2										7					
S1	INT														
D	WORD	D	V											R	
S2	INT		KnX	KnY	KnM	KnS	KnLM		D	SD	C	T	V	Z	R

2

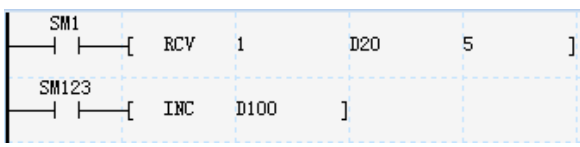
S101SM111SM121RCV

D

S2

1V63D7999D

201



LD SM1

RCV 1 D20 5

LD SM123

INC D100

1RCV

SM1

6.13

6.13.1 CCITT

[CCITT (S1) (S2) (D)]										MC200 MC100 MC80 MC280			
CCITT S1 S2 D										7			
S1	WORD								D			V	R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	Z R
D	WORD								D			V	R

S1

S2

D

1

2

1

CCITT

CCITT

X^12 X^5 1

S1

S2

D

0

X^16

X0

D

D

SM1

[MOV 16#0 0 D0]

[MOV 16#11 17 D1]

[MOV 16#22 34 D2]

[MOV 16#33 51 D3]

[MOV 16#44 68 D4]

[MOV 16#55 85 D5]

[MOV 16#66 102 D6]

[MOV 16#77 119 D7]

[MOV 0 28097 D100]

[CCITT D0 8 28097 D100]

LD SM1

MOV 16#00 D0

MOV 16#11 D1

MOV 16#22 D2

MOV 16#33 D3

MOV 16#44 D4

MOV 16#55 D5

MOV 16#66 D6

MOV 16#77 D7

LD X0

MOV 0 D100

CCITT D0 8 D100

X0=ON

D0

8

CCITT

D100

6.13.3 LRC

[LRC (S1) (S2) (D)]										MC200 MC100 MC80 MC280					
LRC S1 S2 D										7					
S1	WORD								D				V		R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	WORD								D				V		R

S1

S2

D

LRC

1

2

S2 0

S1 S2 D

D

SM1

[

MOV

16#0

D0

]

[

MOV

16#11

D1

]

[

MOV

16#22

D2

]

[

MOV

16#33

D3

]

[

MOV

16#44

D4

]

[

MOV

16#55

D5

]

[

MOV

16#66

D6

]

[

MOV

16#77

D7

]

MO

[

MOV

0

D100

]

[

LRC

D0

8

D100

]

LD SM1

MOV 16#00 D0

MOV 16#11 D1

MOV 16#22 D2

MOV 16#33 D3

MOV 16#44 D4

MOV 16#55 D5

MOV 16#66 D6

MOV 16#77 D7

LD M0

MOV 0 D100

LRC D0 8 D100

X0=ON

D0

8

LRC

D100

6.14

6.14.1 ZRST

[ZRST (D) (S)]										MC200 MC100 MC80 MC280					
ZRST D S										5					
D	BOOL			Y	M	S	LM				C	T			
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

D

S

1

2

C

T

C

T

D

S

SM0

[

ZRST

OFF M10

10

]

LD SM0

ZRST M10 10

SM0=ON

M10

M10

M11

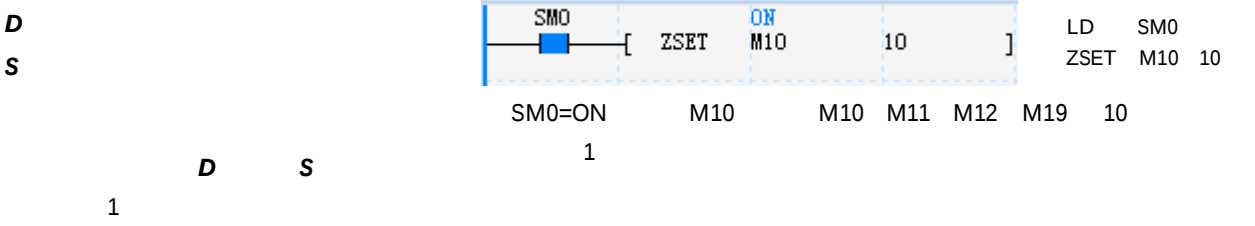
M12

M19

10

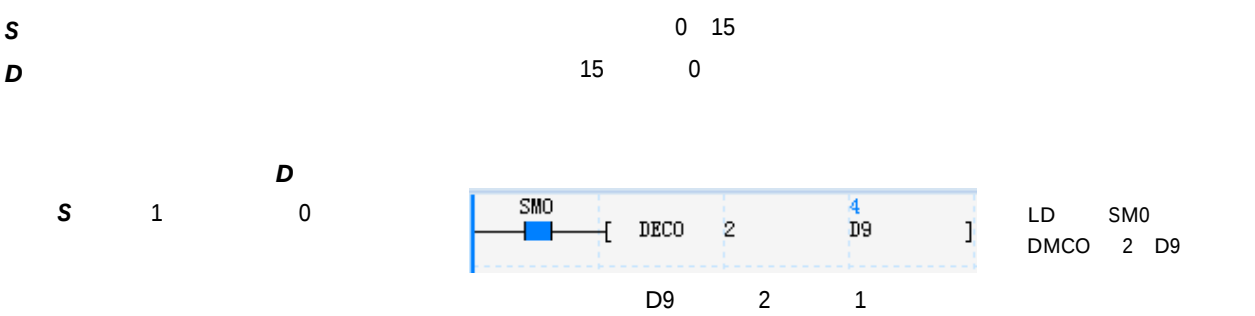
6.14.2 ZSET

ZSET												MC200 MC100 MC80 MC280					
ZSET D S												5					
D	BOOL			Y	M	S	LM				C	T				✓	
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	✓	

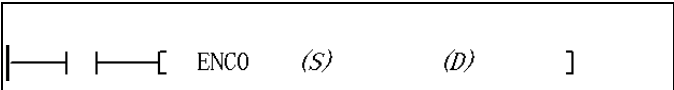


6.14.3 DMCO

 DECO (S) (D)										MC200 MC100 MC80 MC280					
DMCO S D										5					
S	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	INT			KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

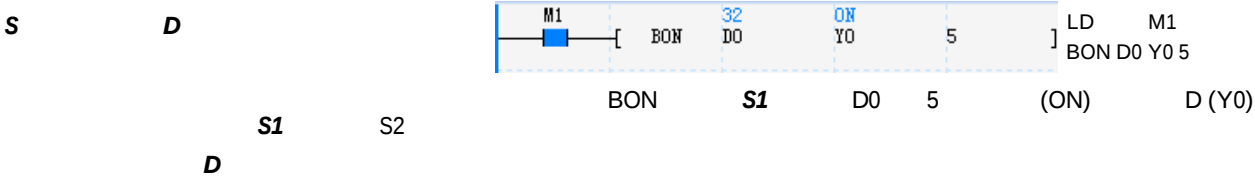


6.14.4 ENCO

										MC200 MC100 MC80 MC280					
ENCO S D										5					
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	Z	R

6.14.7 BON ON

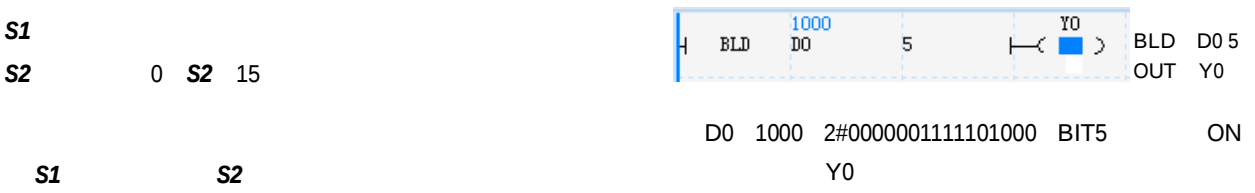
										MC280						
BON S1 D S2										7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V			
D	BOOL		Y	M	S											
S2	INT								D				V		R	



6.15

6.15.1 BLD LD

										MC200 MC100 MC80 MC280						
BLD S1 S2										5						
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	



6.15.2 BLDI LDI

												MC200 MC100 MC80 MC280					
———— BLDI (S1) (S2) —()																	
BLDI S1 S2												5					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		

S1

S2

0

S2

15

LDI

D0

5

Y0

BLDI D0 5

OUT Y0

D0 1000 2#0000001111101000 BIT5 ON

OFF

Y0

S1

S2

6.15.3 BAND AND

BLD (S1) (S2) BAND										MC200 MC100 MC80 MC280					
BLD															
BAND S1 S2										5					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R

S1

S2

0

S2

15

LDI

D0

5

Y0

LD X0

BAND D0 5

OUT Y0

1000 2#0000001111101000 BIT5 ON

Y0

S1

S2

6.15.4 BANI ANI

BLDI (S1) (S2) BANI												MC200 MC100 MC80 MC280					
BLDI																	
BANI S1 S2												5					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		

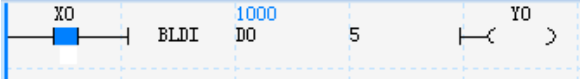
S1

S2

0

S2

15



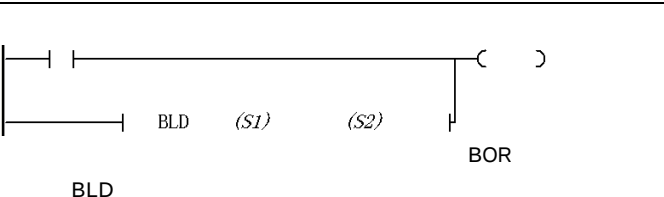
D0 1000 2#0000001111101000 BIT5 ON
X0=ON Y0

LD X0

BANI D0 5

OUT Y0

6.15.5 BOR OR

												MC200 MC100 MC80 MC280					
BOR S1 S2												5					
S1	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R		

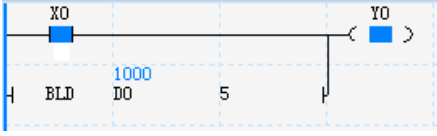
S1

S2

0

S2

15



D0 1000 2#0000001111101000 BIT5 ON
X0=ON Y0

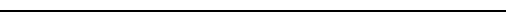
LD X0

BOR D0 5

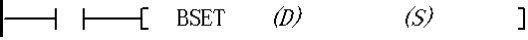
OUT Y0

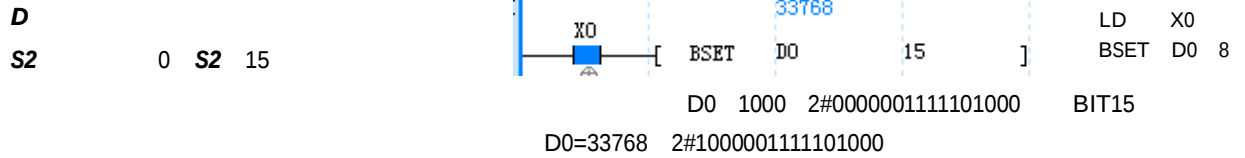
Diagram illustrating a 1000ms timer circuit. The circuit includes a start button (S1), a stop button (S2), a buzzer (Y0), and a timer (T0). The timer is set to 1000ms (1000). The output Y0 is ON when the timer is running and OFF when the timer is done.

6.15.7 BOUT

											MC200 MC100 MC80 MC280					
BOUT D S											5					
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R	
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	

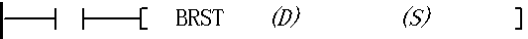
6.15.8 BSET

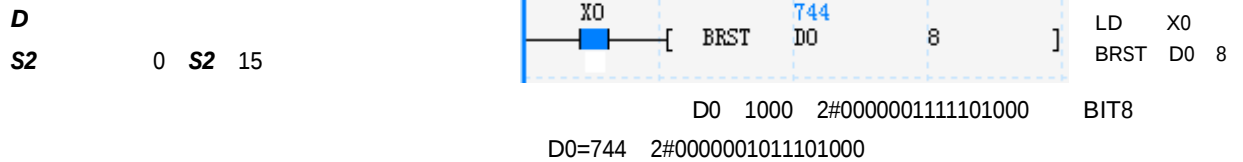
										MC200 MC100 MC80 MC280					
BSET D S										5					
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R



D **S**

6.15.9 BRST

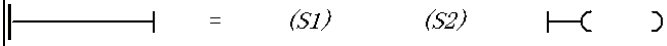
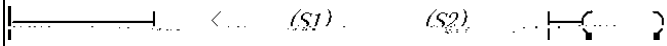
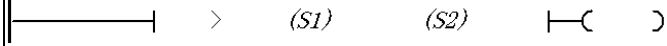
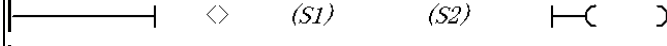
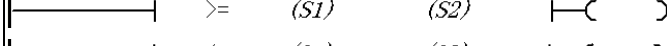
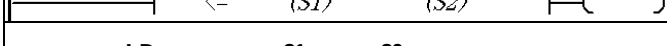
										MC200 MC100 MC80 MC280					
BRST D S										5					
D	WORD			KnY	KnM	KnS	KnLM		D		C	T	V	Z	R
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R



D **S**

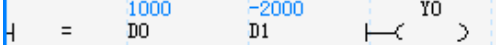
6.16

6.16.1 LD = < > <> >= <= LD

										MC200 MC100 MC80 MC280						
																
																
																
																
																
LD S1 S2										5						
LD S1 S2																
LD S1 S2																
LD S1 S2																
LD S1 S2																
LD S1 S2																
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	

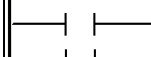
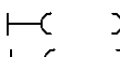
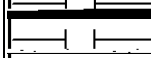
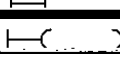
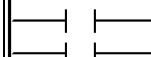
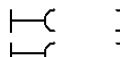
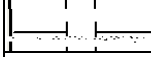
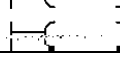
S1 1
S2 2

S1 S2 BIN

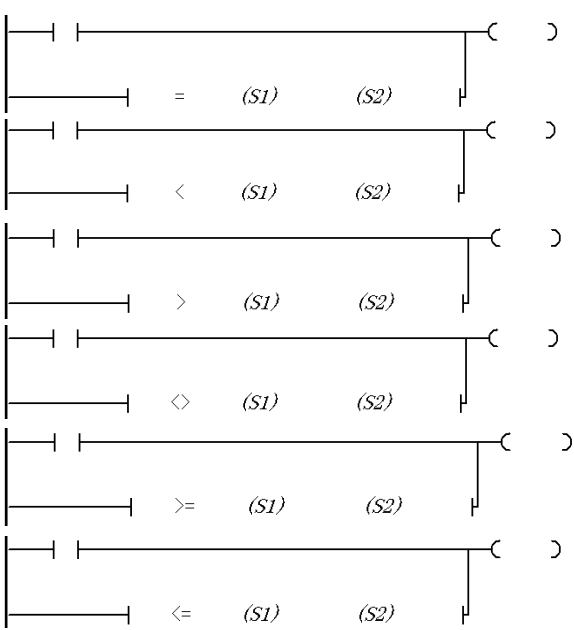
	=	1000 D0	-2000 D1	Y0
	<	1000 D0	-2000 D1	Y1
	>	1000 D0	-2000 D1	Y2
	<>	1000 D0	-2000 D1	Y3
	>=	1000 D0	-2000 D1	Y4
	<=	1000 D0	-2000 D1	Y5
		D0 D1	BIN	

LD= D0 D1
OUT Y0
LD< D0 D1
OUT Y1
LD> D0 D1
OUT 2
LD<> D0 D1
OUT Y3
LD>= D0 D1
OUT Y4
LD<= D0 D1
OUT Y5

6.16.2 AND = < > <> >= <= AND

						MC200	MC100	MC80	MC280
	=	(S1)	(S2)						
	<	(S1)	(S2)						
	>	(S1)	(S2)						
	<=	(S1)	(S2)						
	>=	(S1)	(S2)						
	<=	(S1)	(S2)						
AND S1 S2						5			
AND S1 S2									
AND S1 S2									
AND S1 S2									
AND S1 S2									
AND S1 S2									
S1	INT	KnX	KnY	KnM	KnS				

6.16.3 OR = < > <> >= <= OR



MC200 MC100 MC80 MC280

sh F F . .

6.16.4 LDD = < > <> >= <= LDD

							MC200	MC100	MC80	MC280
		D=	(S1)	(S2)	{	}				
		D<	(S1)	(S2)	{	}				
		D>	(S1)	(S2)	{	}				
		D<>	(S1)	(S2)	{	}				
		D>=	(S1)	(S2)	{	}				
		D<=	(S1)	(S2)	{	}				

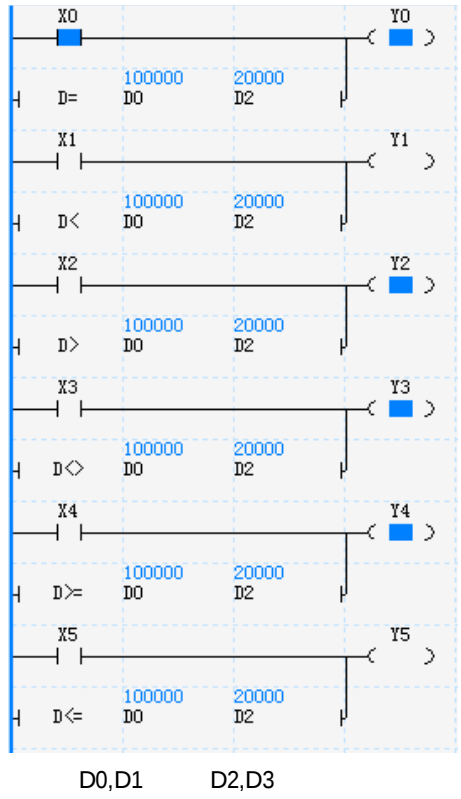
6.16.6 ORD = < > <> >= <= ORD

										MC200 MC100 MC80 MC280					
ORD S1 S2 ORD S1 S2 ORD S1 S2 ORD S1 S2 ORD S1 S2 ORD S1 S2										7					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R

S1 1

S2 2

S1 S2



LD X0

ORD= D0 D2

OUT Y0

LD X1

ORD< D0 D2

OUT Y1

LD X2

ORD<> D0 D2

OUT Y2

LD X3

ORD>= D0 D2

OUT Y3

LD X4

ORD>= D0 D2

OUT Y4

LD X5

ORD<= D0 D2

OUT Y5

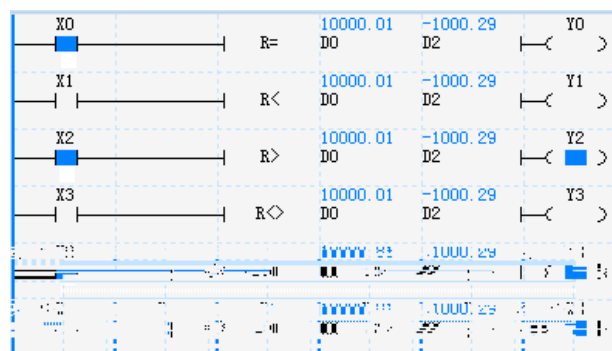
	R=	(S1)	(S2)	H(C)	)		MC200	MC100	MC280
	R<	(S1)	(S2)	H(C)	)				
	R>	(S1)	(S2)	H(C)	)				
	R<>	(S1)	(S2)	H(C)	)				
	R>=	(S1)	(S2)	H(C)	)				
	R<=	(S1)	(S2)	H(C)	)				

6.16.8 ANDR

										MC200 MC100 MC280						
		R=	(S1)	(S2)												
		R<	(S1)	(S2)												
		R>	(S1)	(S2)												
		R<>	(S1)	(S2)												
		R>=	(S1)	(S2)												
		R<=	(S1)	(S2)												
ANDR		S1	S2	7												
ANDR		S1	S2													
ANDR		S1	S2													
ANDR		S1	S2													
ANDR		S1	S2													
ANDR		S1	S2													
S1	REAL								D				V		R	
S2	REAL								D				V		R	

S1	1
S2	2

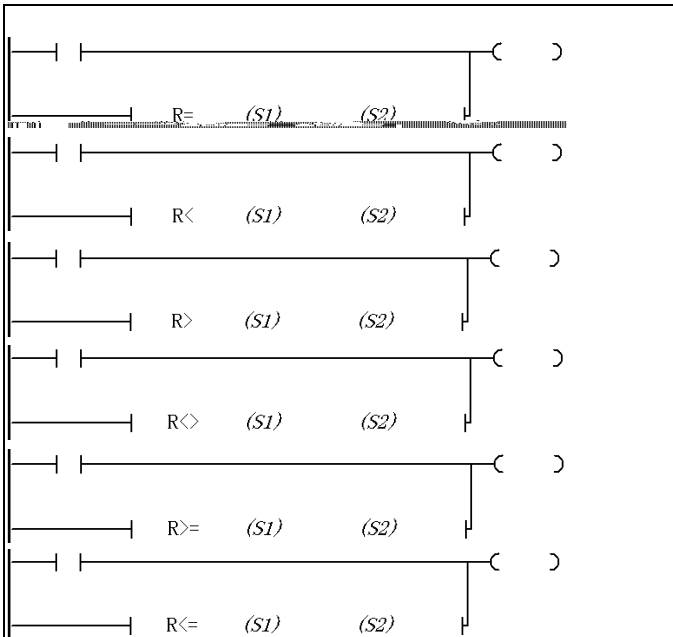
S1 S2



LD	X0
ANDR=	D0 D2
OUT	Y0
LD	X1
ANDR<	D0 D2
OUT	Y1
LD	X2
ANDR<>	D0 D2
OUT	Y2
LD	
ANDR<>	Y3
LD	X4
ANDR>=	D0 D2
OUT	Y4
LD	X5
ANDR<=	D0 D2
OUT	Y5

D0,D1 D2,D3

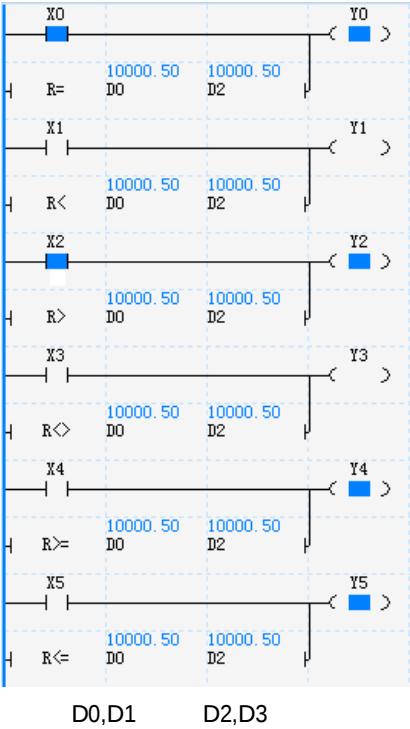
6.16.9 ORR

										MC200 MC100 MC280					
ORR S1 S2 ORR S1 S2 ORR S1 S2 ORR S1 S2 ORR S1 S2 ORR S1 S2										7					
S1	REAL								D				V		R
S2	REAL								D				V		R

S11

S22

S1S2



LDX0

ORR=D0D2

OUTY0

LDX1

ORR<D0D2

OUTY1

LDX2

ORR>D0D2

OUTY2

LDX3

ORR<>D0D2

OUTY3

LDX4

ORR>=D0D2

OUTY4

LDX5

ORR<=D0D2

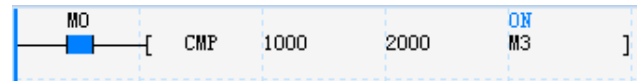
OUTY5

6.16.10 CMP

									MC200 MC280							
CMP S1 S2 D									7							
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	Z	R	
D	BOOL			Y	M	S										

S1
S2
D

S1 S2
D D+1 D+2 ON

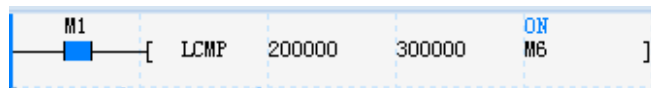


6.16.11 LCMP

									MC200 MC280							
LCMP S1 S2 D									9							
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V	Z	R	
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V	Z	R	
D	BOOL			Y	M	S										

S1 1
S2 2
D

D D+1 D+2 ON



S1 S2

6.16.12 RCMP

---	--	--	--	--	--	--	--

6.17.2 BKSUB

									MC280					
[BKSUB (S1) (S2) (D) (S3)]														
BKSUB (S1) (S2) (D) (S3)									9					
S1	INT								D	SD	C	T	V	R
S2	INT								D	SD	C	T	V	R
D	INT								D	SD	C	T	V	R
S3	INT								D				V	R

S1

S2

D

S3:

1

2

M1	[BKSUB 1 D10 30 D100 ~29 D1000 5]													
----	-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	--	--

LD M1
BKSUB D10 D100 D1000 5
M1=ON D10 5 D100
5
D1000 5 D1000=D10-D100
D1001=D11-D101 D1004=D14-D104

6.17.3 BKCMP=,>,<,<>,<=,>=

---	--	--	--	--	--	--	--	--

S1

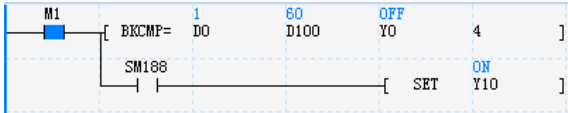
S2

D

S3:

1

2 S1 16 ,S1
S1 S2 s3 16
D S3
3 D S3 ON
SM188



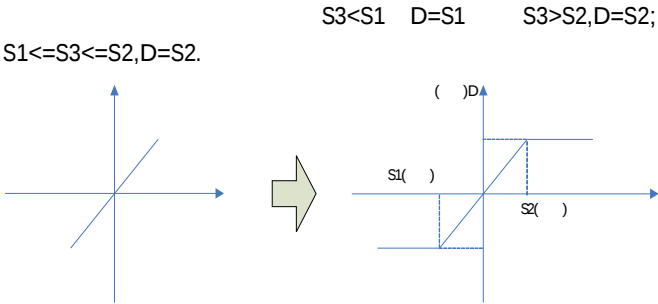
LD M1
BKCMP= D10 D100 Y0 4
LD SM188
SET Y10
M1=ON D10 4 D100
4 Y0
4 ON Y10
ON

6.18

6.18.1 LIMIT

									MC280						
LIMIT (S1) (S2) (S3) (D)															
LIMIT (S1) (S2) (S3) (D)									9						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S1
S2
S3
D:



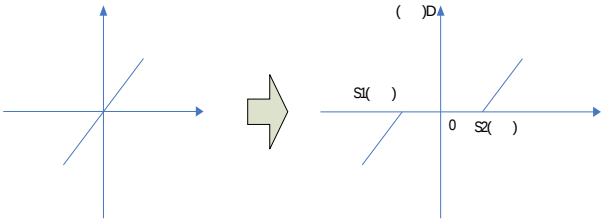
M1	10	100	30	30
	D0	D10	D100	D1000

LD M1
LIMIT D0 D10 D100 D1000

6.18.2 DBAND

										MC280					
DBAND (S1) (S2) (S3) (D)															
DBAND (S1) (S2) (S3) (D)										9					
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S1
S2
S3
D:



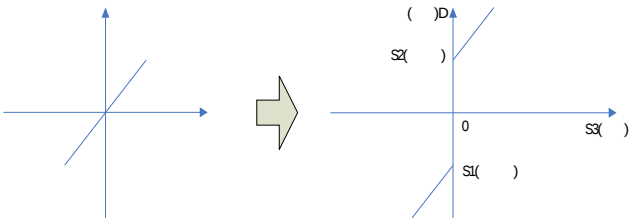
LD M1
DBAND D0 D10 D100 D1000

S3<S1 D=S3-S1
S3>S2,D=S3-S2; S1<=S3<=S2,D=0.

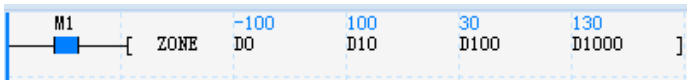
6.18.3 ZONE

										MC280					
ZONE (S1) (S2) (S3) (D)															
ZONE (S1) (S2) (S3) (D)										9					
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S3	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S1
S2
S3
D:



ZONE D0 D10 D100 D1000



LD M1

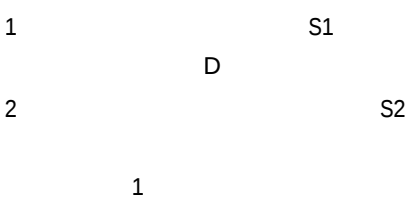
6.18.4 SCL

										MC280						
SCL (S1) (S2) (D)																
										7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R		
S2	INT								D				V	R		
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R		

S1

S2

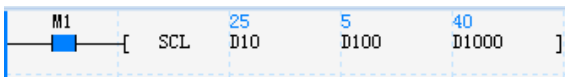
D:



		S2
1	X	S2+1
	Y	S2+2
2	X	S2+3
	Y	S2+4
ë	ë	ë
n ()	X	S2+2n-1
	y	S2+2n

1 X

2 S1



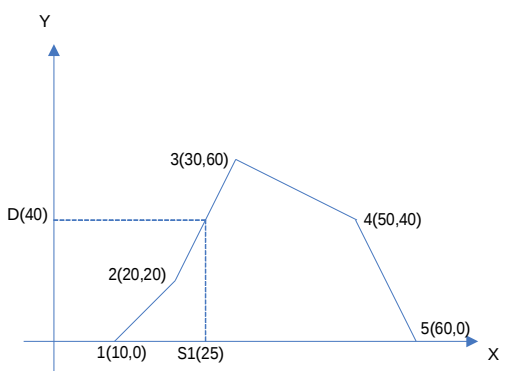
LD M1

SCL D10 D100 D1000

M1=ON D10

D1000

		D100	5
1	X	D101	10
	Y	D102	0
2	X	D103	20
	Y	D104	20
3	X	D105	30
	y	D106	60
4	X	D107	50
	y	D108	40
5	X	D109	60
	y	D110	0



6.18.5 SER

									MC280						
SER (S1) (S2) (D) (S3)]															
SER (S1) (S2) (S3) (D)									9						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	
S3	INT								D				V	R	

S1 1. S1 S3 , S2
S2 ,

D

S3: 1 S3
256

6.19

6.19.1 STRADD

									MC280						
STRADD (S1) S2 D									7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
S2	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S1
S2
D:

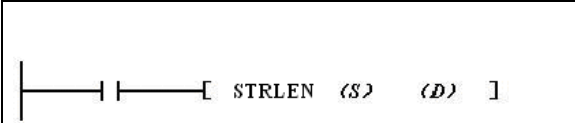
1

F Õ!y#“” é

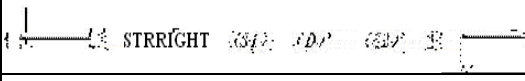
S1 S2

D

6.19.2 STRLEN

		MC280
STRLEN S D		5

6.19.3 STRRIGHT

										MC280					
STRRIGHT S1 D S2										7					
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	
S2	INT								D				V	R	

S1

D

S2

1

2

3

4

1 S1

2 S2

3 S2

00H

0

S1

S1

D

00H

0000H

M1

[STRRIGHT D10 D100 3]

LD M1

STRRIGHT D10 D100 3

M1=ON D10

D100

B15---b8 b7---b0

D10

D11

D12

D13

0x32

0x31

0x34

0x33

0x36

0x35

0x00

0x00

B15---b8 b7---b0

D100

D101

0x35

0x34

0x00

0x36

6.19.4 STRLEFT

									MC280						
STRLEFT S1 D S2									7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	
S2	INT								D				V	R	

S1
D
S2

1

m

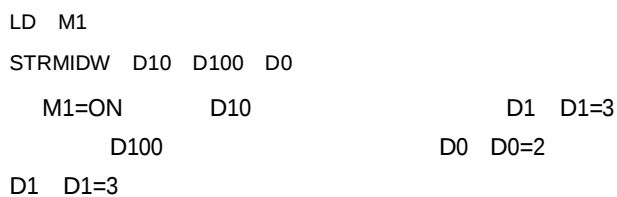
% .



6.19.5 STRMIDR

									MC280						
STRMIDR S1 D S2									7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S1				1	S2		S1	
D				2	n	-2		
S2				3	S2		1	
S2+1		n		4				D
1		S1	n	5	S1,D			00H
	D		S2					
	n							

MC

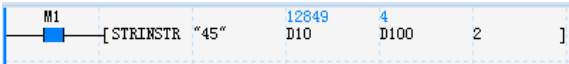
6.19.7 STRINSTR

[STRINSTR (S1) (S2) (D) (S3)]											MC280					
STRINSTR S1 S2 D S3											9					
S1	INT								D	SD	C	T	V	R		
S2	INT								D	SD	C	T	V	R		
D	INT								D	SD	C	T	V	R		
S3	INT								D				V	R		

2 S3 S2
3 S1 32 ,

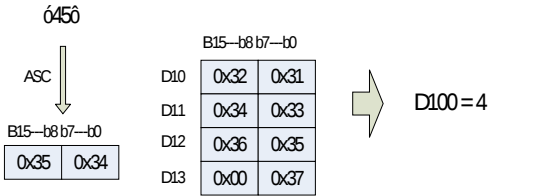
S1
S2
D
S3:
4 S1 00H S2
00H S2
00H

1 S2 S3
S1
D
2 D 0
3 S3 0
4 00H



LD M1
STRINSTR "45" D10 D100 2
M1=ON D10 2
45 D100

1 S1 S2
00H

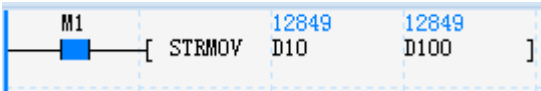


6.19.8 STRMOV

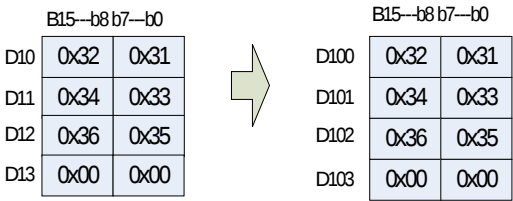
									MC280						
STRMOV (S) (D)									5						
S	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T	V	R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C	T	V	R	

S
D:

1 S 00H
D ;
2
00H
1 S 00H
2 S 00H
D 00H
3 S1 32 ,



LD M1
STRMOV D10 D100
M1=ON D10 D100



6.20

6.20.1 ZRN

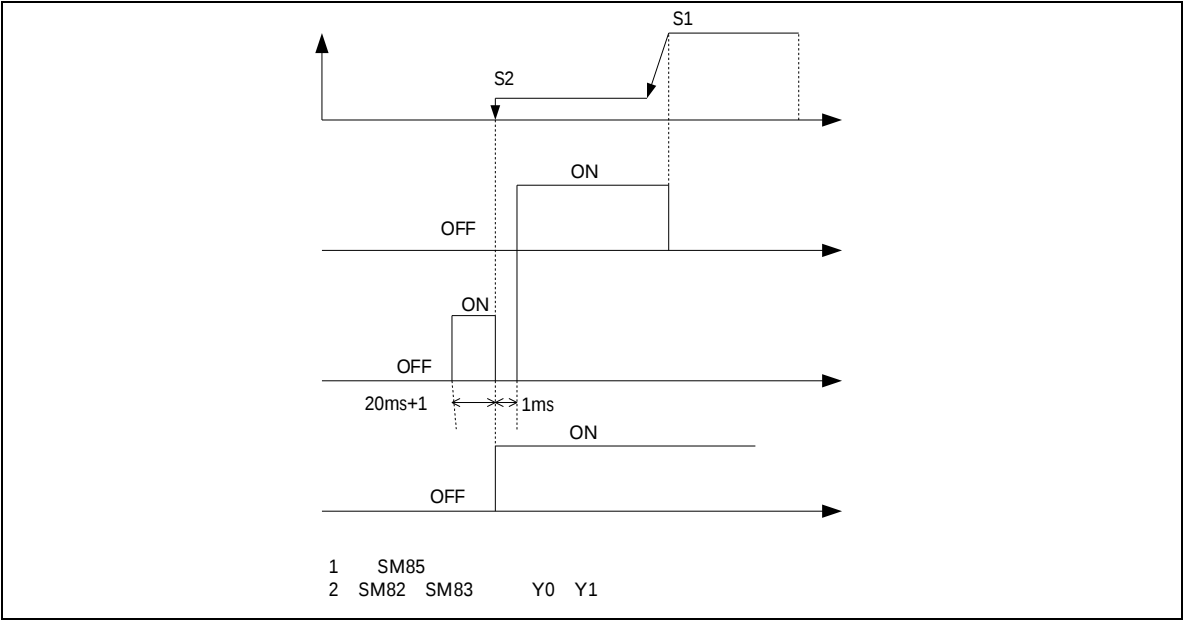
										MC200 MC100 MC280						
ZRN S1 S2 S3 D										11						
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R	
S3	BOOL		X	Y	M	S										
D1	BOOL			Y												

F_{min_acc}

S1																
32	MC100	MC200	10	100000	Hz				4							
MC280	10	200000	Hz							SD84					SD87	
S2																
				DOG	ON					SD85						
										SD84						
S3																
				X					0		0					
									0							
PLC																
										SD84					PLC	
D																
					MC100	MC200,				SD84		100				
	Y0	Y1		MC280,		Y0	Y1		5							
Y2	Y3	Y4	Y5	Y6	Y7					SD80/SD82						
										SD80/SD82						
SM85																
							Y0			SD80/SD82						
Y1					Y2	Y3	SM85			SM82/SM83				SD80/SD82		
			Y2	Y3										Y0/Y1		
4																
MC200	MC280			SD		MC100			6	SD50/SD52					PLC	
															SD50/SD52	
5																
				ZRN											SD80/SD82	
7																
										SD			MC100	MC200/MC280		
										SD			MC100			
2																

$$F_{min_acc} = \sqrt{\frac{F_{max} \cdot 500}{T}}$$

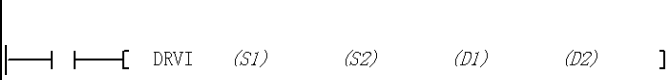
F_{max} SD85 SD86
 T SD87



6.20.2 PLSV

[PLSV (S) (D1) (D2)]										MC200 MC100 MC280		
PLSV S D1 D2										8		
S	DINT	KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	V	R

6.20.3 DRVI

										MC200 MC100 MC80 MC280					
DRVI S1 S2 D1 D2										11					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D1	BOOL			Y											
D2	BOOL			Y	M	S									

S1

32 999999 999999

S2 Hz

32 MC100 MC200 10 100000 Hz MC280

10 200000 Hz

D1 MC100 MC200,
Y0 Y1 MC280, Y0 Y1 Y2

Y3 Y4 Y5 Y6 Y7

D2**S1**

4

● **S1** D2 ON● **S1** D2 OFF

1

S1

● Y0 SD80 SD81 32

● Y1 SD82 SD83 32

2

3

S1

4

5

OFF

SM

6

OFF

SM80,SM81

ON

7. SM440 SM441 SM443 Y0/Y1 Y2/Y3

Y6/Y7 AB ON AB OFF

OFF

7

SD

SD

MC100

MC100 MC200/MC280

MC200 MC280 SD MC100 ,

$$F_{\min_acc} = \sqrt{\frac{F_{\max}}{T} \cdot 500}$$

 $F_{\max}$ T

SD85 SD86

SD87

 $F_{\min_acc}$

6.20.4 DRVA

 DRVA (S1) (S2) (D1) (D2)										MC200 MC100 MC280					
DRVA S1 S2 D1 D2										11					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		R
D1	BOOL			Y											
D2	BOOL			Y	M	S									

S1

32 999999 999999

S2

Hz
32 MC100 MC200 10 100000 Hz MC280
10 200000 Hz

D1

MC100 MC200,
Y0 Y1 MC280, Y0 Y1 Y2
Y3 Y4 Y5 Y6 Y7
PLC

D2

D2 ON D2 OFF

1 S1

● Y0 SD80 SD81 32
● Y1 SD82 SD83 32

2
3 S1
4

5 OFF
SM
6 OFF
SM80 SM81 ON

7. SM440 SM441 SM443 Y0/Y1 Y2/Y3
Y6/Y7 AB ON AB OFF
OFF

MC200 MC280 SD MC100 ,

$$F_{min_acc} \sqrt{\frac{F_{max}}{T} \frac{500}{T}}$$
$$F_{max}$$
$$T$$

SD85 SD86
SD87

 F_{min_acc}

4
SD84 SD87
SD85
SD84 0
0 0
SD84
PLC SD84
100
5
SD80/SD82
SD80/SD82 SD80/SD82
SM82/SM83
SD80/SD82
Y0/Y1
6 SD50/SD52 PLC
SD50/SD52
SD80/SD82

7 SD MC100 MC200/MC280
SD MC100

6.20.5 ABS

ABS (S) (D1) (D2)												MC200 MC100 MC280					
ABS S D1 D2												8					
S	BOOL	X	Y	M	S												
D1	BOOL		Y	M	S												
D2	DINT		KnY	KnM	KnS					D	SD	C			R		

- S

5 ABS

ON

ABS

S,S 1,S 2 3 X

6

ABS

32 6

D1

7 ABS bit0 bit1 2

8 79

D2

32

80

D2 1 2

ABS

SD80 SD82 32

SD80 SD82
- 1 PLC

PLC
- 2 ABS

D2

SD80

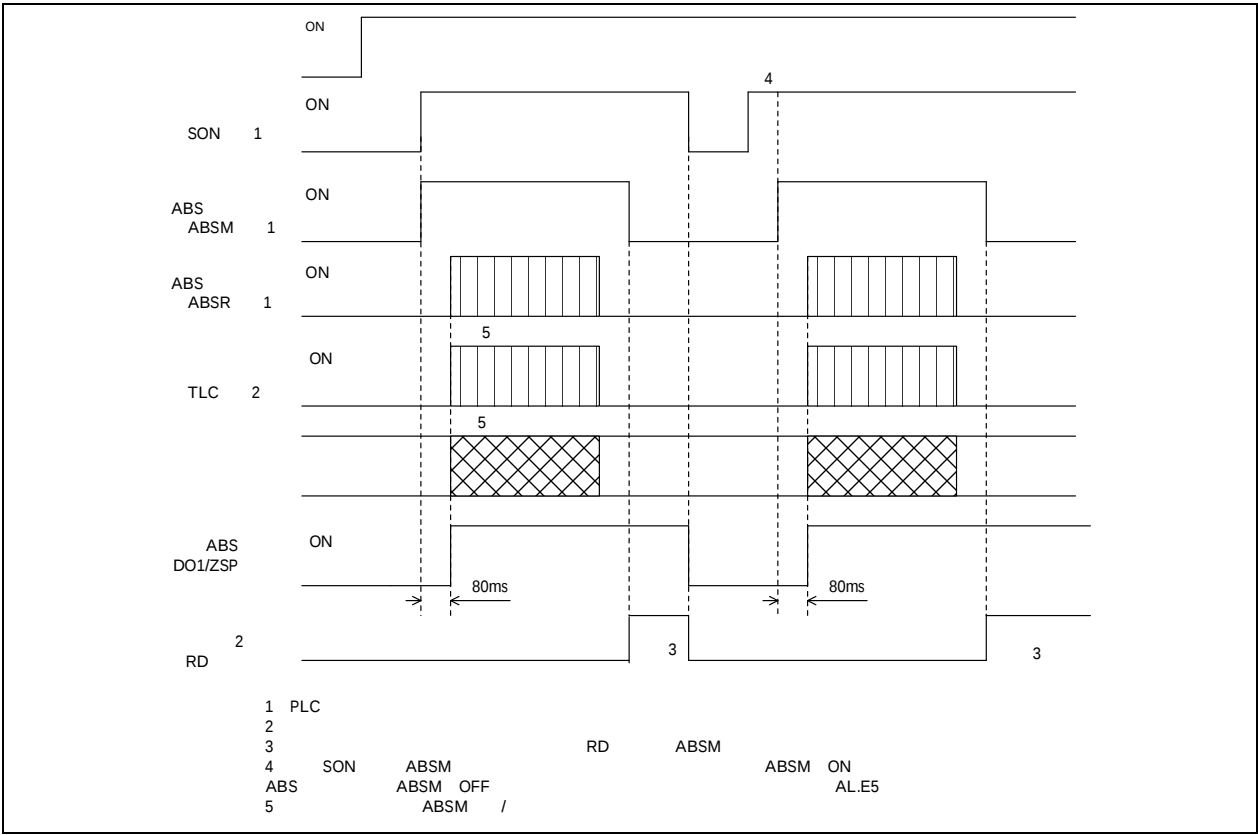
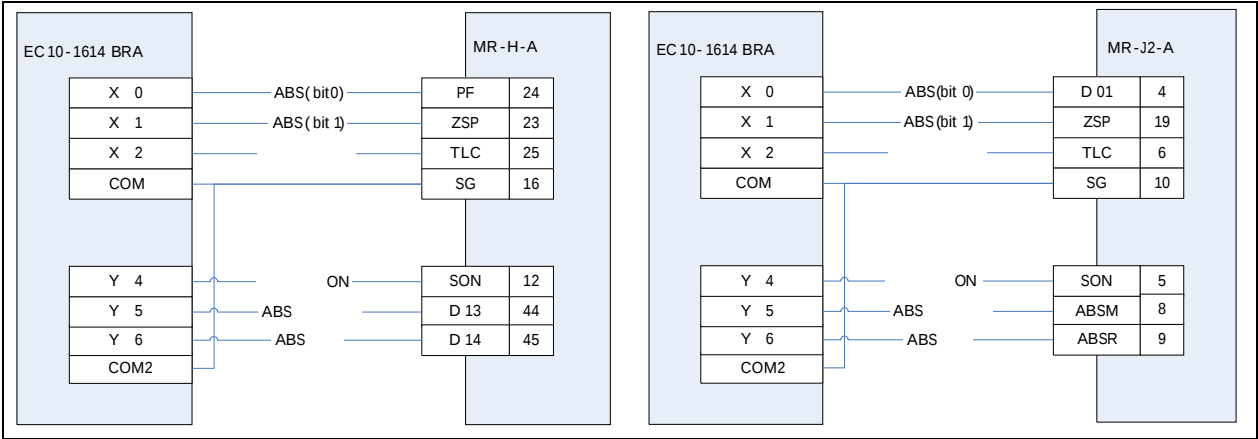
SD82
- 3 ABS

ABS

ABS

ON OFF
- 4 SM82 SM83 Y0 Y1
5. MC200 MC280 SD MC100 ,

ABS



ABS

MR J2 MR J2S

ABS

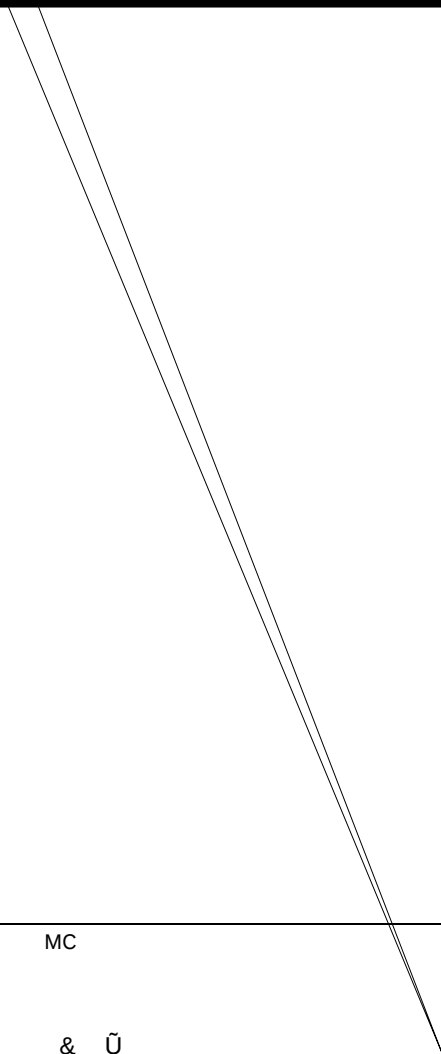
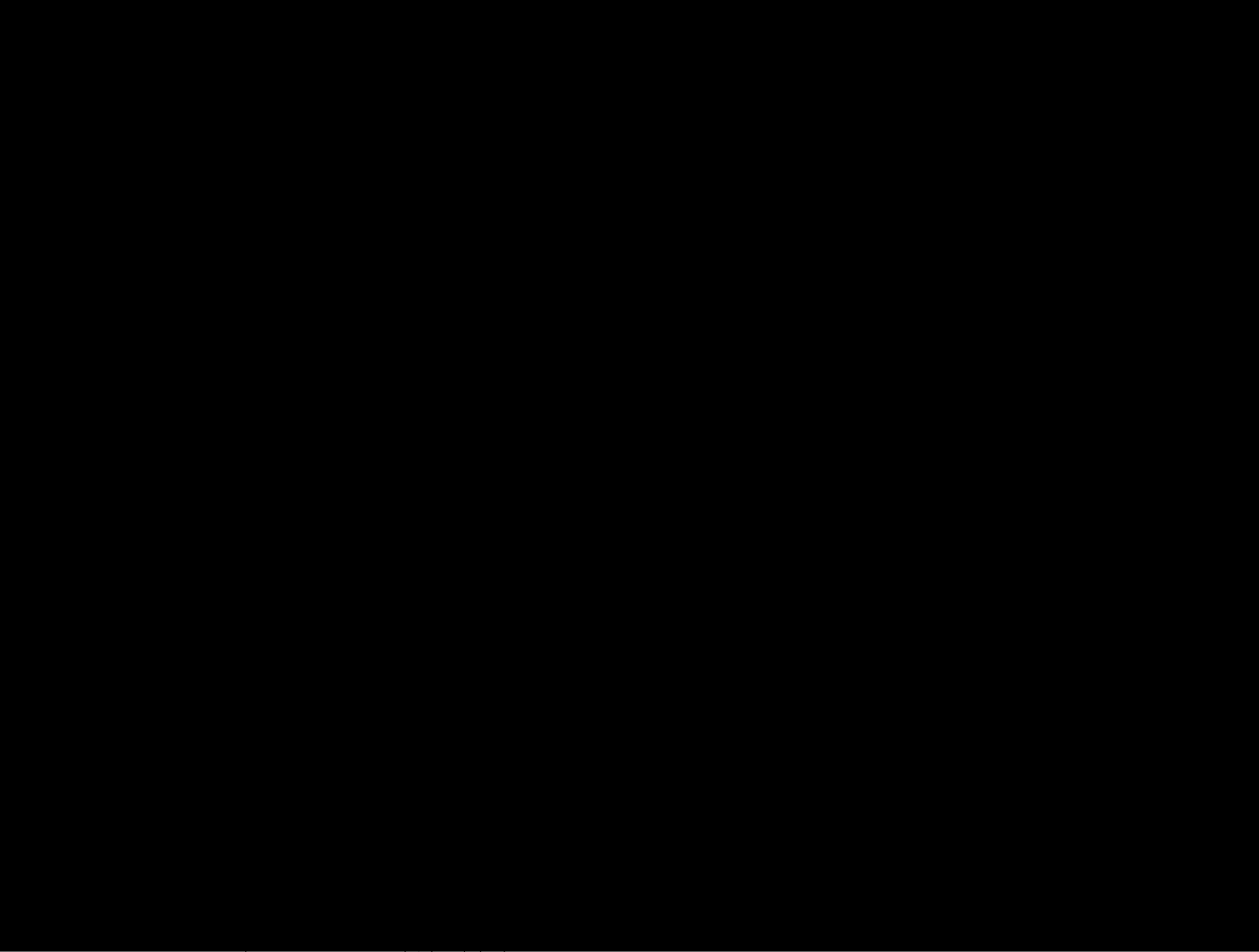
32

ABS

ABS

6.20.6 DSZR DOG

						MC200 MC280	
[DSZR]							
DSZR (S1) (S2) (D1) (D2)						9	



MC

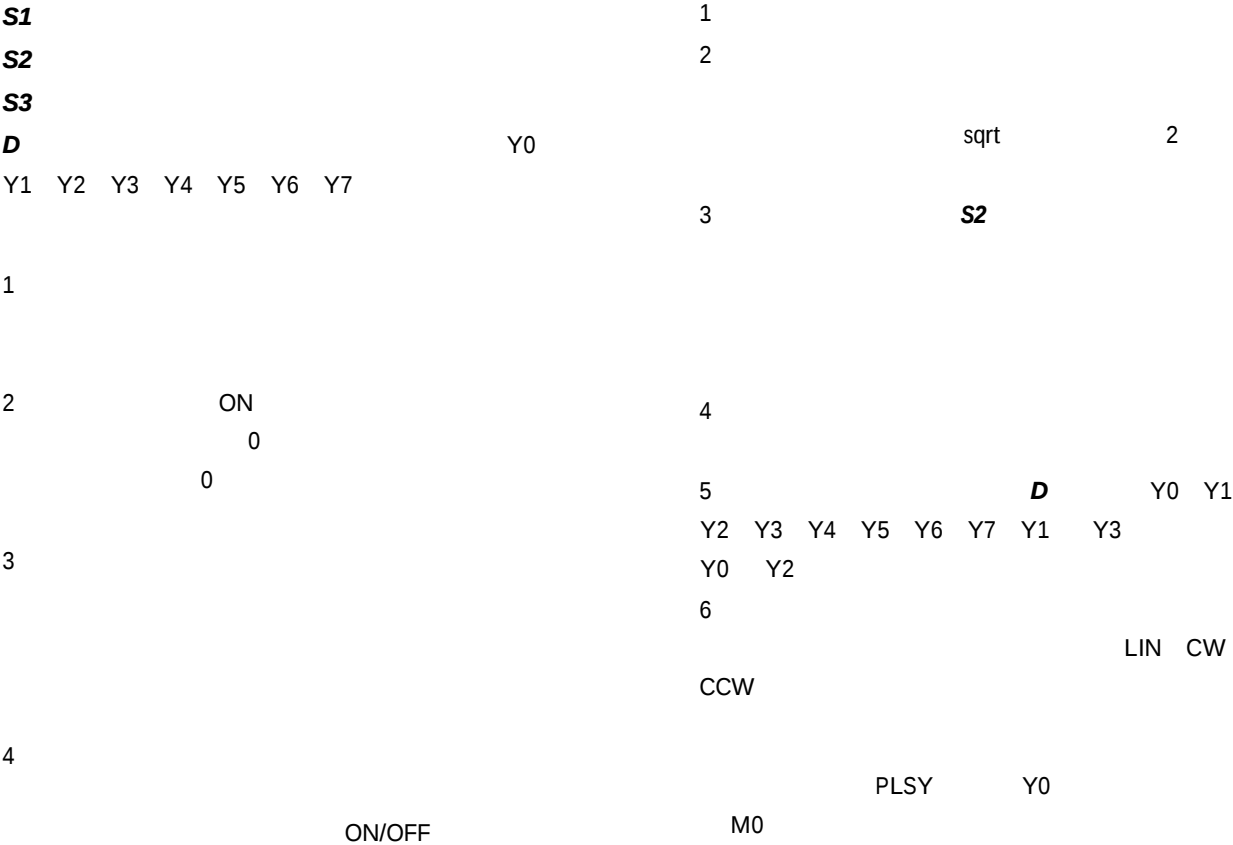
S0	[	DMOV	100000	100000	SD202	]
	[	MOV	100	100	SD204	]
	[	MOV	5000	5000	SD205	]
	[	MOV	2000	2000	SD207	]
	[	MOV	8000	8000	SD208	]

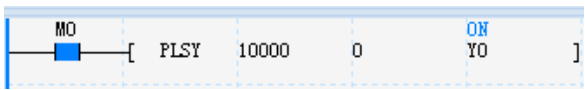
DOG

M8	[	DSZR	OFF	OFF	OFF	OFF	]
			M100	X0	Y0	Y4	

6.20.7 STOPDV

[STOPDV]										MC280					
STOPDV S1 S2 S3 D										12					
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S3	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
D	BOOL			Y											





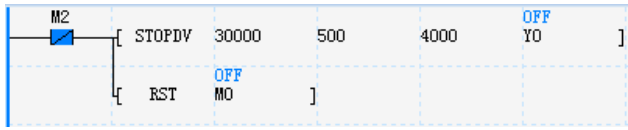
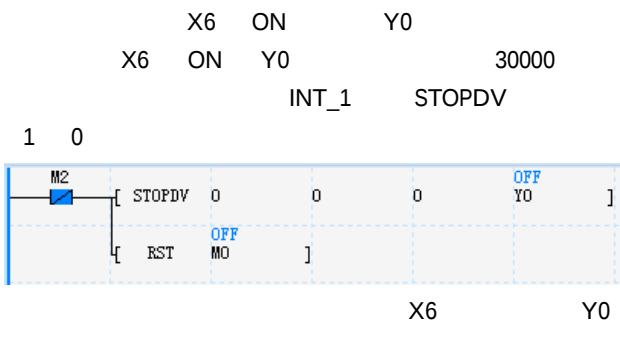
INT_1

程序名称: 作者:

中断事件: ...

程序说明:

确定 取消



6.20.8 LIN

LIN										MC280					
LIN S D1 D2 D3 D4										12					
S	DINT									D					
D1	BOOL			Y											
D2	BOOL			Y											
D3	BOOL			Y											
D4	BOOL			Y											

D			
	10		
S+1			
	00		ON/ OFF
	01		+
	10		<u>2</u>

S

D1

D2

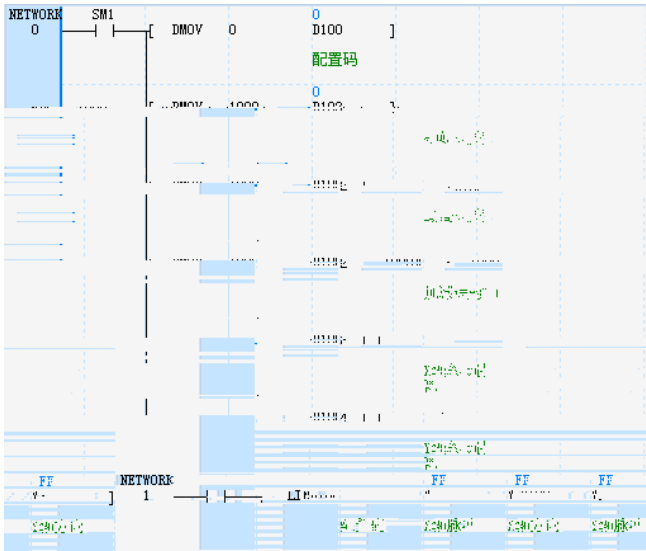
D3

D4



D	
S	

1
Y0 Y2 Y1 Y3 Y0 Y2
D1 D3 Y4,Y5,Y6,Y7 2
2 Y0 Y2 +
+ 100k Y4 Y5
Y6 Y7 +
20k
3 16,777,215
4



6.20.9 CW

								
CW								
CW	S	D1	D2	D3	D4			
S	DINT							D
D1	BOOL		Y					
D2	BOOL		Y					
D3	BOOL		Y					
D4	BOOL		Y					

S

D1

D2

D3

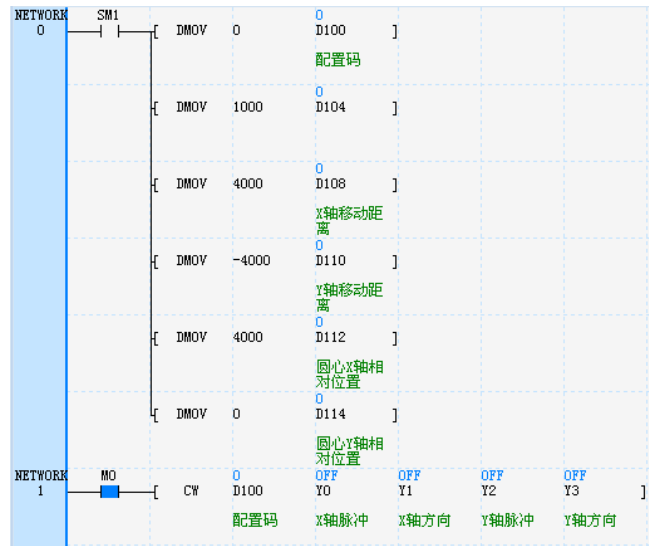
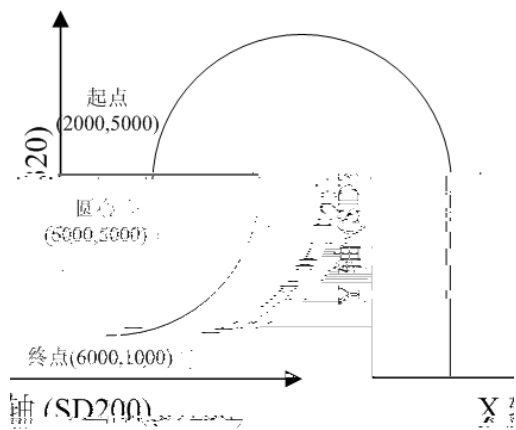
D4 < Õ73B* D

1

2 Ê

Ê

D			
S			
	0		
	1		
S+1			
	00		ON/
	01		+
	10		ON/
	11		+
S+2			
S+3			
S+4			
S+5			
S+6			
S+7			
S+8	X		
S+9	X		
S+10	Y		
S+11	Y		
S+12	X	/	X
S+13	X	/	X
S+14	Y	/	



6.20.10 CCW

CCW										MC280									
CCW										12									
S	DINT									D									
D1	BOOL			Y															
D2	BOOL			Y															
D3	BOOL			Y															
D4	BOOL			Y															

S

D1

D2

D3

D4

1

2

D	
S	
0	
1	

D	
S+1	10
	00
	01
	10
	11
S+2	
S+3	
S+4	
S+5	
S+6	
S+7	
S+8	X
S+9	X
S+10	Y
S+11	Y
S+12	X / X
S+13	X / X
S+14	Y / Y
S+15	Y / Y

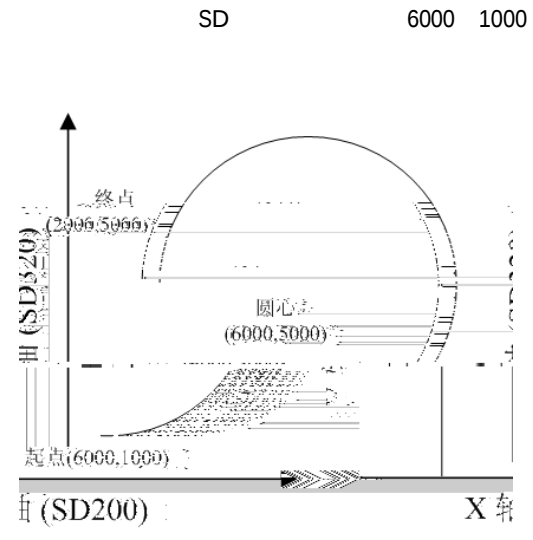
1

X Y

2

X Y

1
Y0 Y2 D1 D3 Y0 Y2
D1 D3 Y4,Y5,Y6,Y7 2
2 Y0 Y2 +
+ 100k Y4 Y5
Y6 Y7 +
20k
3 16,777,215
4
5



6.20.11 MOVELINK

MOVELINK								MC280							
MOVELINK S1 S2 S3 S4 S5 S6								17							
S1	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S2	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S3	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S4	DINT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C		V		
S5	BOOL			Y											
S6	BOOL			Y							C				

6.20.12 GEARBOX

						MC280				
GEARBOX					D1	S1	D2	S2		9

6.20.13 DRVC

[DRVC (S1) (D1) (S2) (D2)]										MC280					
DRVC (S1) (D1) (S2) (D2)										9					
S1	BOOL										C				
D1	DINT								D						
S2	BOOL			Y											
D2	DINT								D						

t = SD205*(f-sd204)/(SD202-SD204)

S1

2. s (t/1000) *(f+SD204)

D1

3. Y0 SM80

(D1+2 Y SM

(D1+4

4.

5.

S2

6. Y0 SM82 ON

D2

OFF

7. Y0~Y7

1. Y

X

2. Drvi

1. SD205 SD205 SD202(32

) SD204 16 f

SM1	[	DMOV	100000	100000	D0	]		
	[	DMOV	100000	100000	D2	]		
	[	DMOV	150000	141072	D4	]		
SMD	[	HCNT	0	100000	D0	]		
M10	[	DRVC	OFF	100000	D0	OFF	OFF	Y4
			C236			Y0		

6.20.14 CAMTABLE

[CAMTABLE (S1) (S2) (S3) (S4) (S5)]									MC280						
CAMTABLE (S1) (S2) (S3) (S4) (S5)									11						
S1	INT								D	SD	C		V		
S2	DINT								D	SD	C		V		
S3	INT								D	SD	C		V		
S4	INT								D	SD	C		V		
S5	INT								D	SD	C		V		

S1:

S2:

S3:

S4:

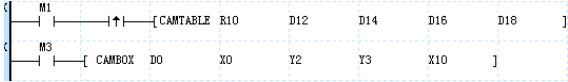
S5:

M1																
M3																

6.20.15 CAMBOX

[CAMBOX (S1) (D1) (D2) (D3) (D4)]										MC280					
CAMBOX (S1) (D1) (D2) (D3) (D4)										9					
S1	INT			Y					D	SD	C		V		
D1	BOOL	X	Y								C				
D2	BOOL		Y												
D3	BOOL		Y	M											
D4	BOOL		X												

S1	CAMTABLE		1								
D1	X0~X7	Y0~Y7	2	C	hcnt						
	C236~C307										
D2	Y0~Y7										
D3	Y0~Y7										
D4	X0~X7										



1.

Table0

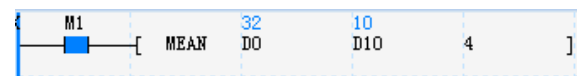
6.21

6.21.1 MEAN

									MC280						
MEAN (S1) (D) (S2)									7						
S1	INT		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T		R	
D	INT			KnY	KnM	KnS	KnLM		D	SD	C			R	
S2	INT								D					R	

S1 1
S2 2
D

1



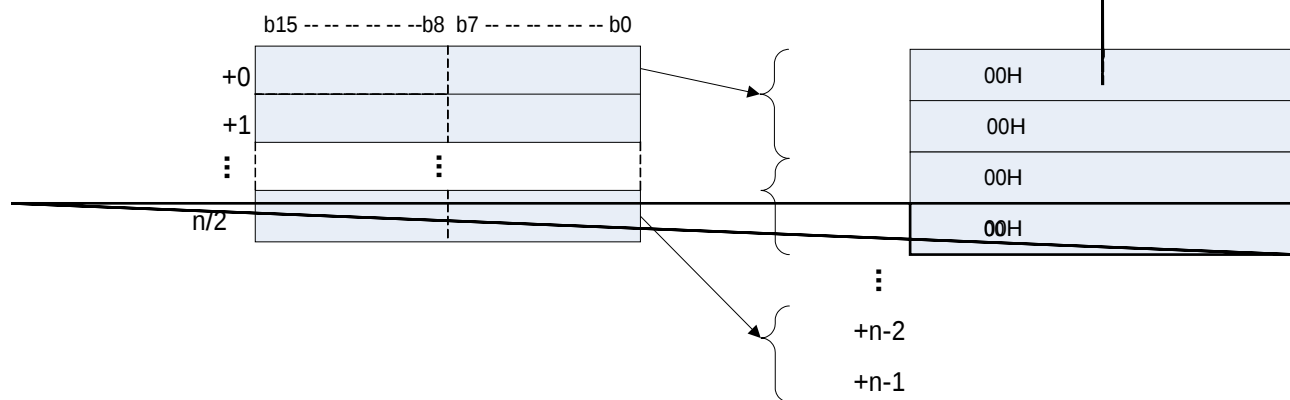
LD M1
 MEAN D0 D10 4
 M1=ON D0 4 ,
 D10 D0=32 D1=10 D2=15 D3=-14
 D10=10

6.21.2 WTOB

									MC280						
WTOB (S1) (D) (S2)									7						
S1	INT								D	SD	C	T		R	
S2	INT								D	SD	C	T		R	
D	INT								D					R	

S1 1
S2 2
D

1

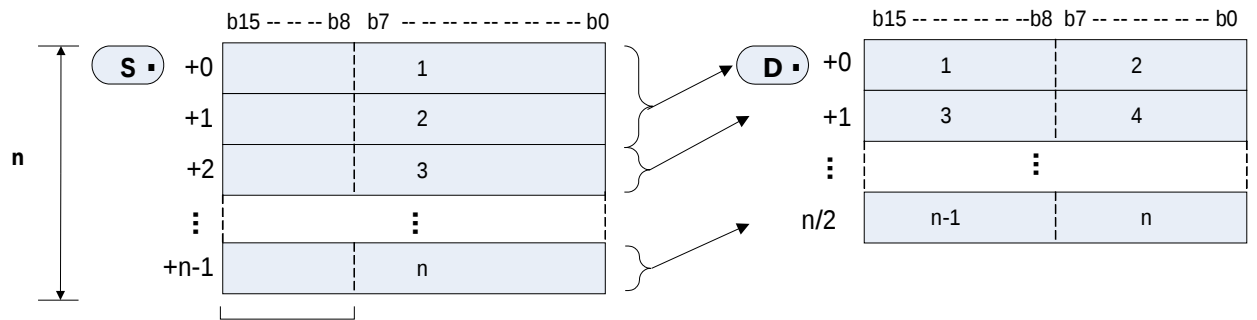


6.21.3 BTOW

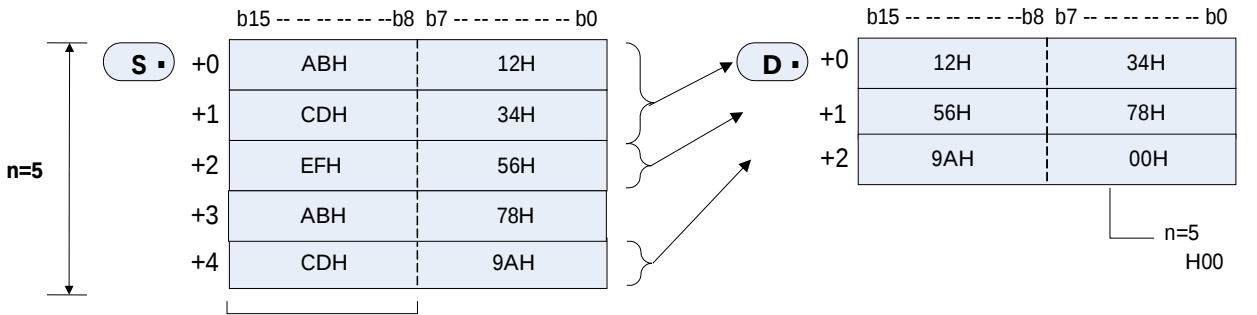
										MC280					
BTOW (S1) (D) (S2)										7					
S1	INT									D	SD	C	T		R
S2	INT									D	SD	C	T		R
D	INT									D					R

S1 1
S2 2
D

1

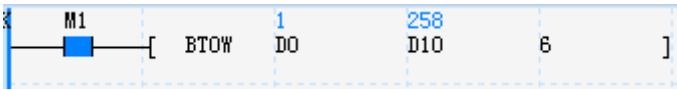


2



3

4



LD M1
BTOW D0 D10 6
M1=ON D0 6 3 D10 3 D0=0x01, D1=0x02,
D2=0x03, D3=0x04, D4=0x05, D5=0x06 D10=0x102, D11=0x304, D12=0x506

6.21.4 UNI

$\vdash \vdash [\text{UNI} \quad (S1) \quad (D) \quad (S2)]$

6.21.5 DIS

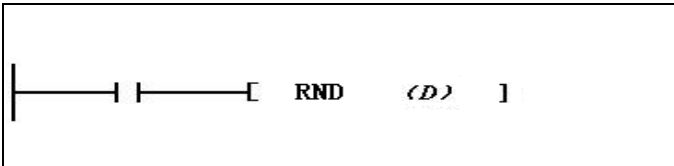
												MC280							
[DIS (S1) (D) (S2)]																			
DIS (S1) (D) (S2)														7					
S1	INT								D	SD	C	T			R				
S2	INT								D	SD	C	T			R				
D INT																D		R	

6.21.6 ANS

[ANS (S1) (S2) (D)]		MC280
(S1) (S2) (D)		7

6.22

6.22.1 RND

										MC280					
RND D										3					
D	WORD		KnX	KnY	KnM	KnS	KnLM	KnSM	D	SD	C	T		Z	R

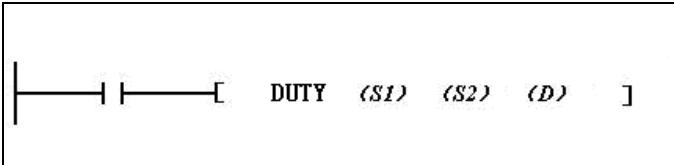
D

1 0 ÷ 32767
D 0
SM180



LD X0
RND D0
M1=ON D0 D0=26406

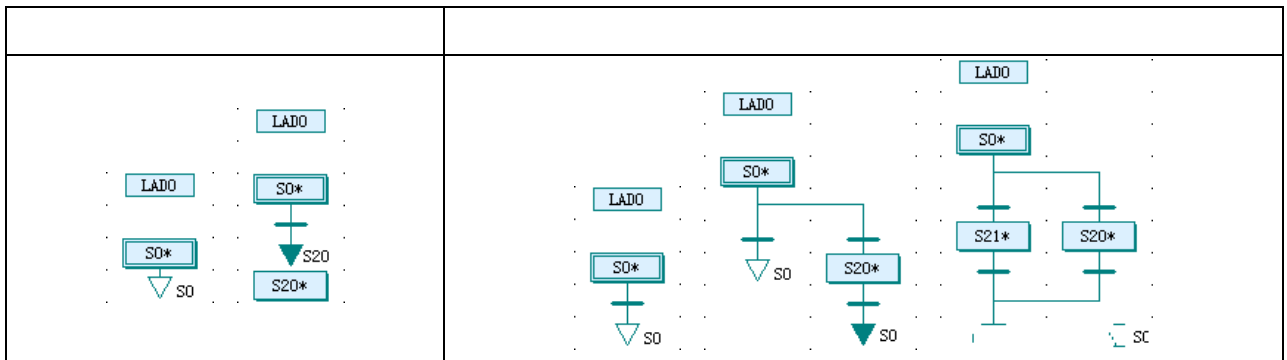
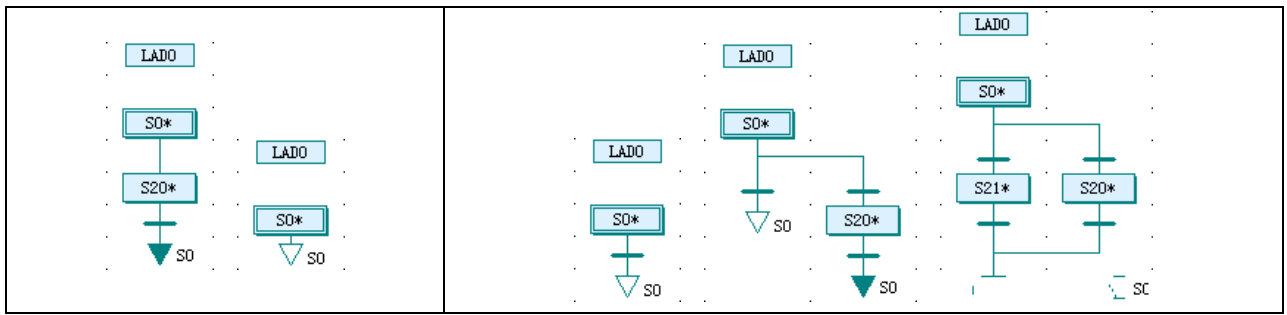
6.22.2 DUTY

										MC280					
DUTY S1 S2 D										7					

7.1		255
TM ^{1.1}		255
7.1.2		255
7.1.3		255

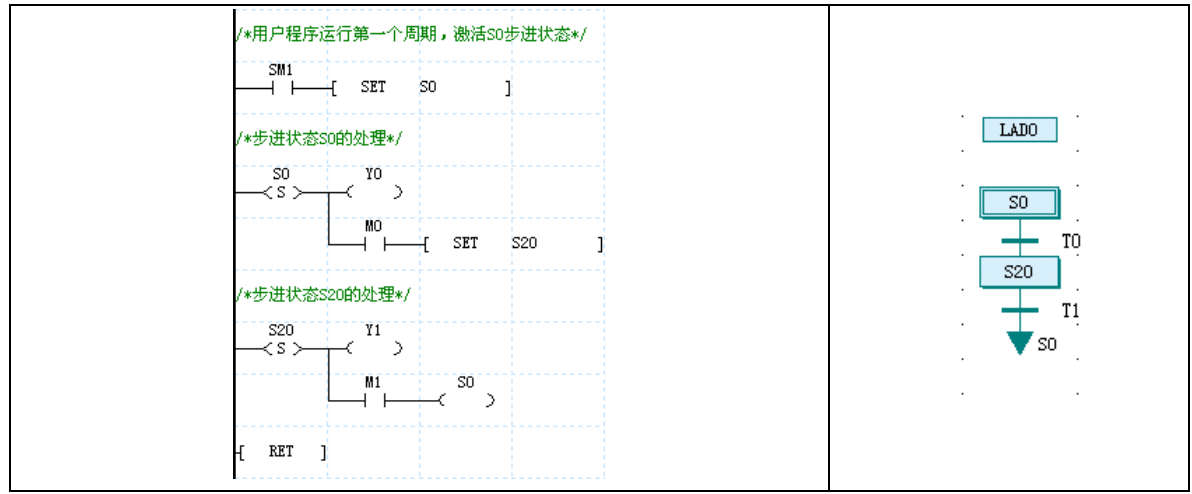
		S
		S ON
		S OFF

--	--



7.1.5

SFC



1.

S ON

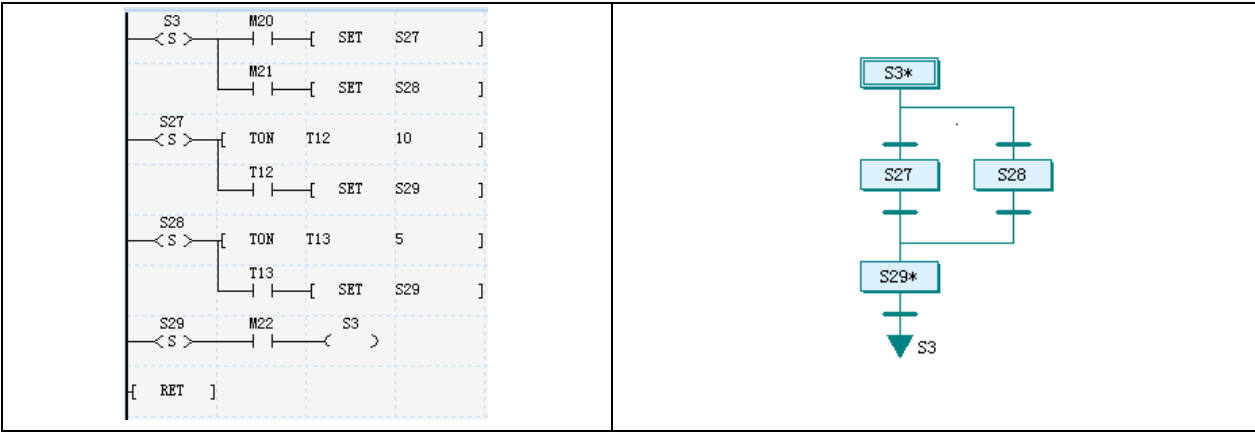
2.

S 0 19

3.

S20991MC200201023MC100

4.



1.

M20M21

M20M21

N0S27S28

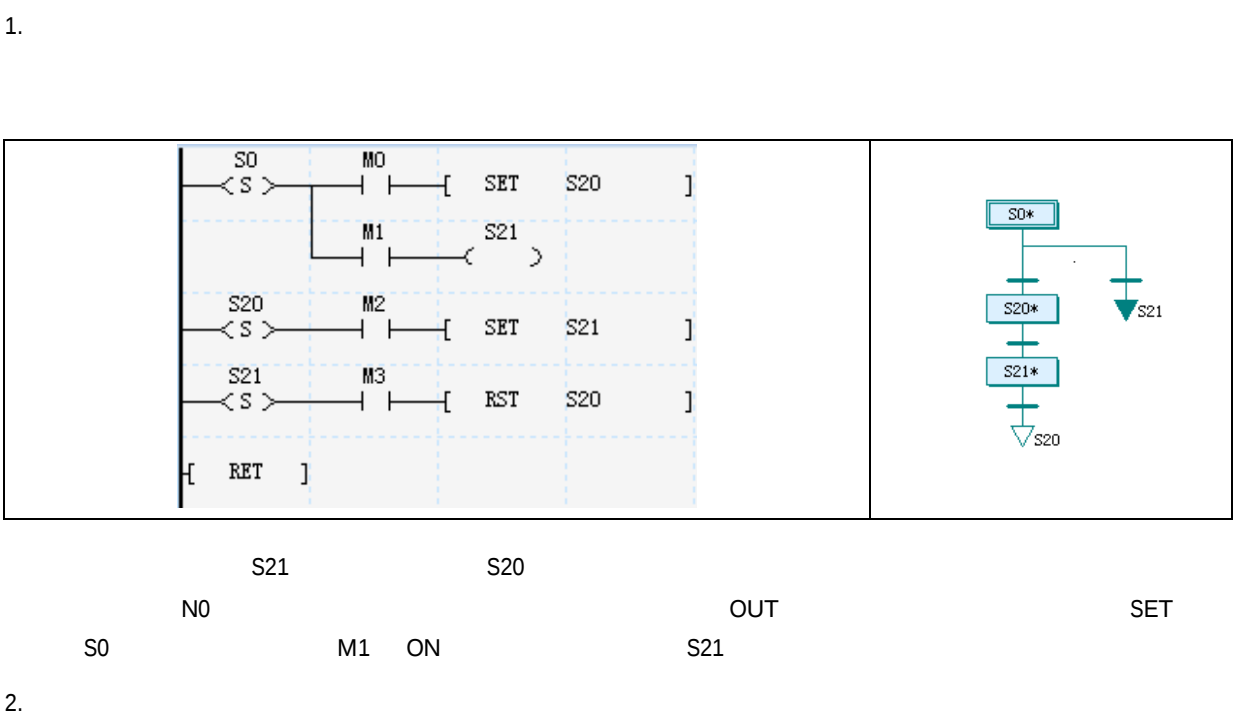
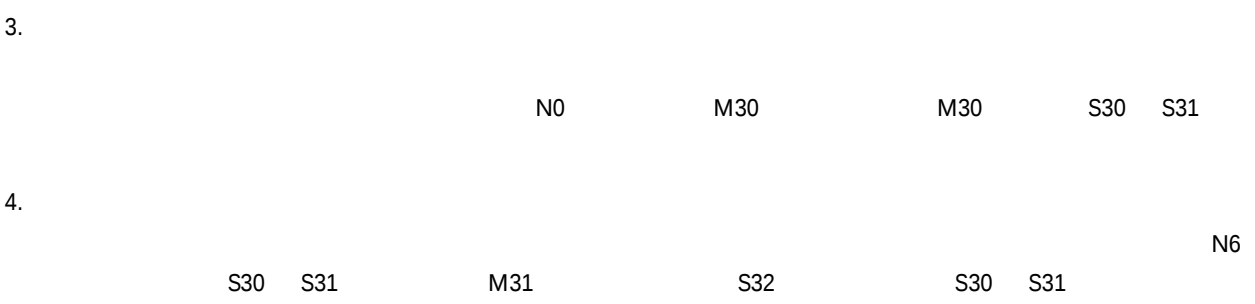
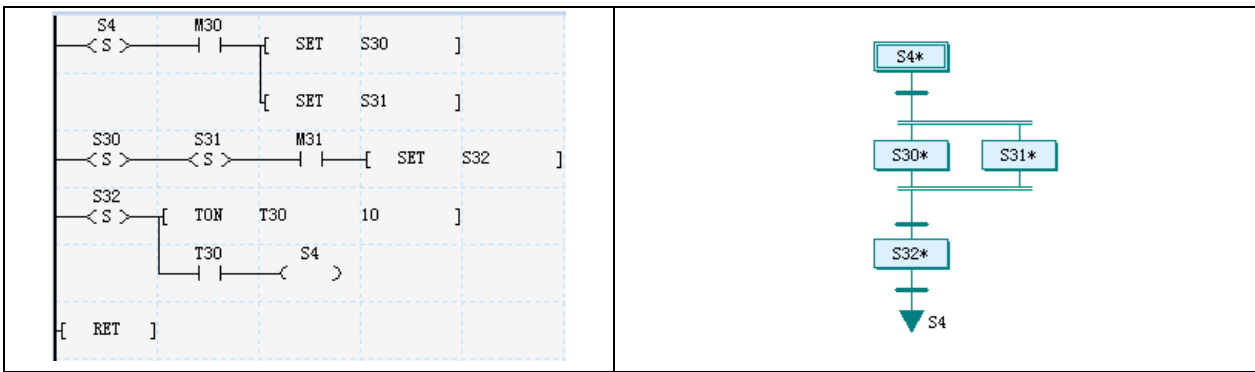
S27S28

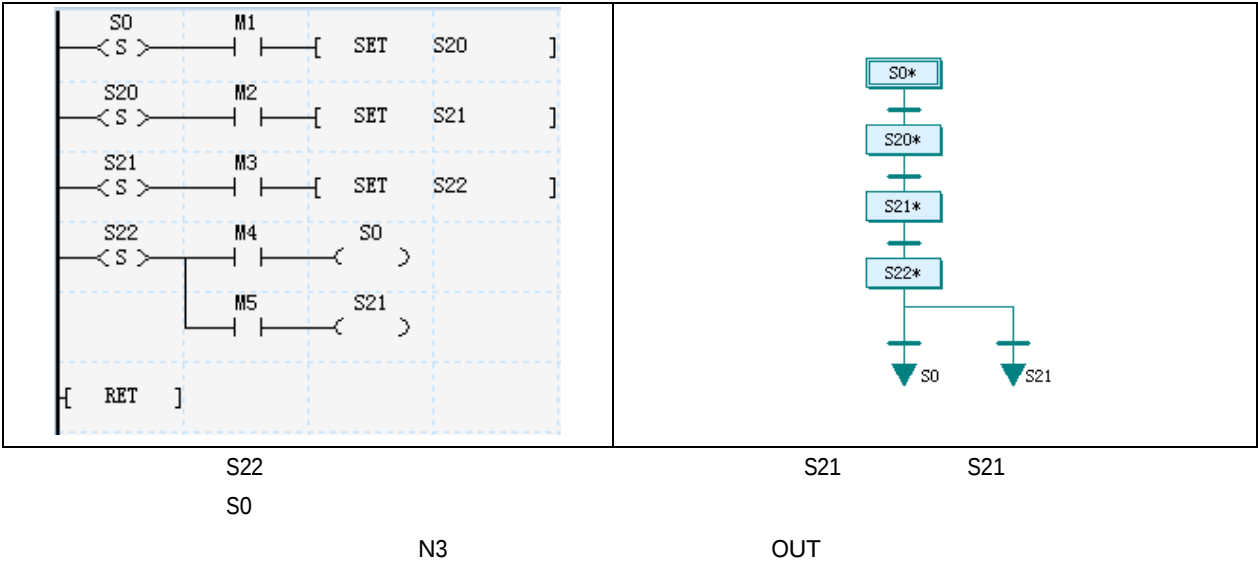
2.

T12N2S28

T13N1S27

S29





M5

|

[

S21

>

[

RET

]

S22

S0

S21

S21

N3

OUT

S0*

|

S20*

|

S21*

|

S22*

|

S0

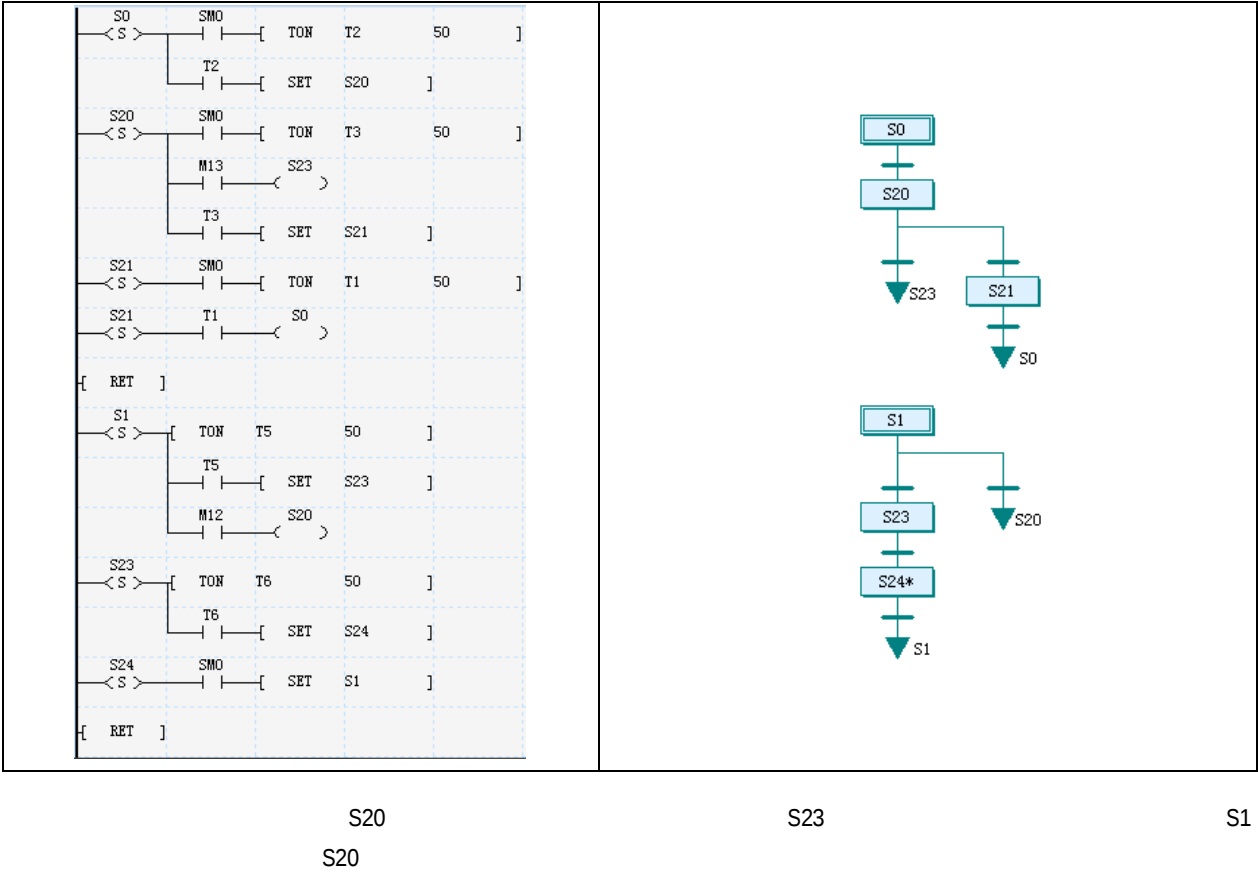
|

S21

3.
MC PLC



PLC



[

RET

]

S1

< S >

TON

T5

50

]

T5

|

[

SET

S23

]

M12

|

[

S20

>

S23

< S >

TON

T6

50

]

T6

|

[

SET

S24

]

S24

< S >

SM0

|

[

SET

S1

]

[

RET

]

S20

S20

S23

S1

S0

|

S20

|

S23

|

S21

|

S0

S1

|

S23

|

S24*

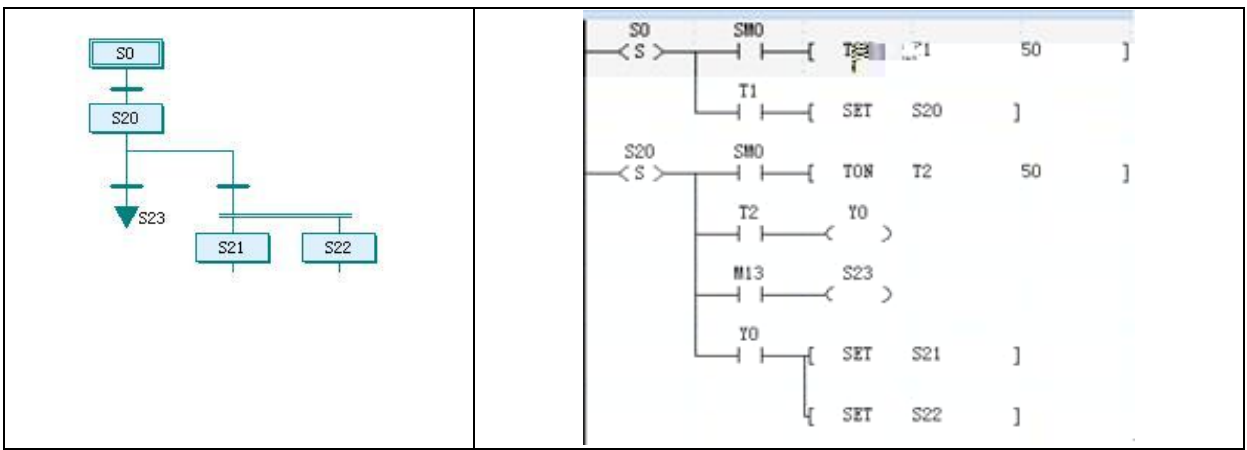
|

S1

OFF S0 S20 S21 OFF S20 S23 S20

7.1.6

T2 S21 S22 M13 OFF S20 S23 T2



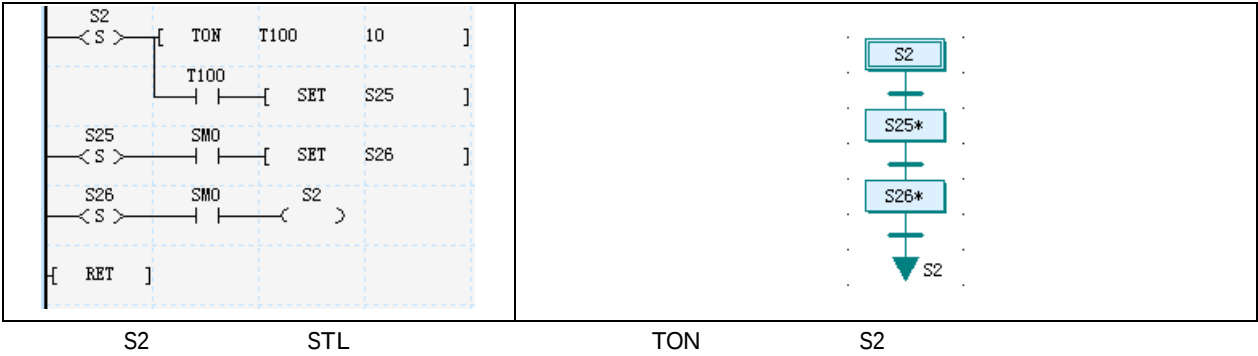
S	ON	OFF	ON/OFF	S
5.3.1 STL SFC				
MC	PLC	S	PLC	
S				
7.4				

7.2

SFC SFC SFC

7.2.1 STL

STL S SFC



STL 5.3.1 STL SFC ON OFF

OUT TON TOF PWM HCNT PLSY PLSR DHSCS SPD DHSCI DHSCR DHSZ DHST

DHSP BOUT

PLC

ON OFF 7.4.1

7.2.2 SFC

SFC

SET

7.2.3 RET SFC

SFC S2 2 S2 SFC

RET

7.2.4 SFC

S2 N3 OUT

S26 N3 RST S26

7.2.5 SFC

7.1.5

7.1.5

7.3

1. SFC

2.

3. SFC
X_Builder SFC SFC PLC

4.

5. SFC SFC

6.



SFC

7.4

STL PLC SFC

7.4.1

1
2 S0-S19
3 RET
4 ON OFF
5
6
7
8
9
10
11

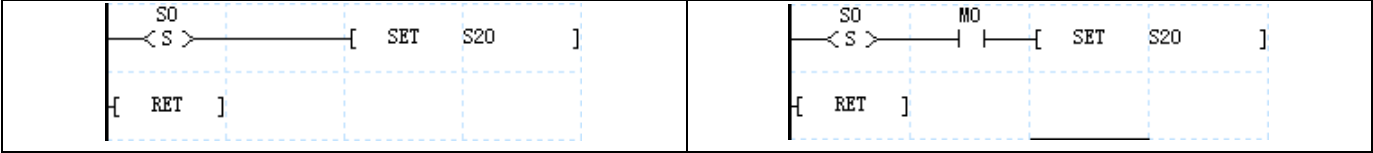
1. PLC S

2. S0-S19
SFC S0-S19 , S20

3. RET
SFC RET

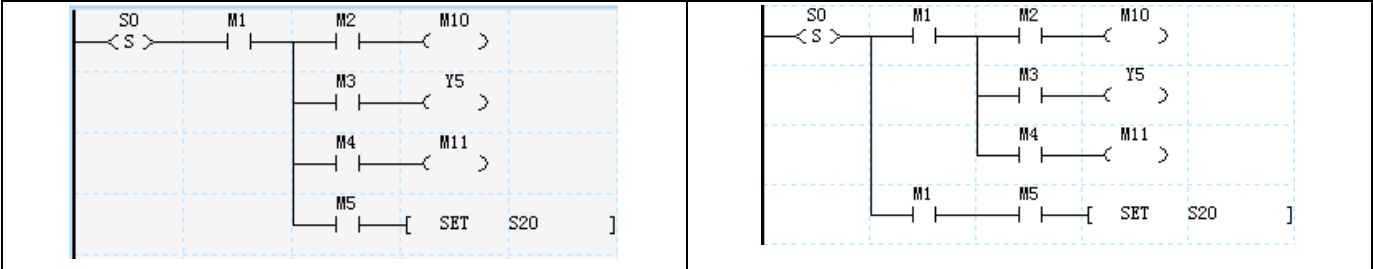
4. ON OFF
ON OFF OUT TON TOF PWM HCNT PLSY PLSR DHSCS SPD DHSCI
DHSCR DHSZ DHST DHSP BOUT

5.

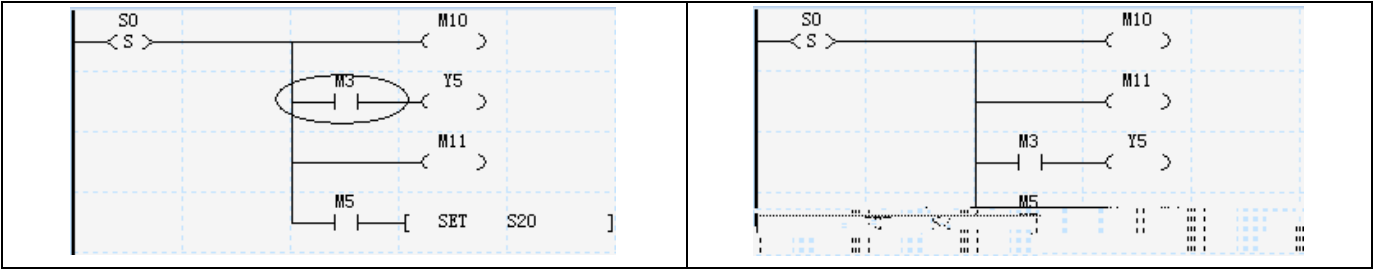


6.

M1



7.



8.

PLC

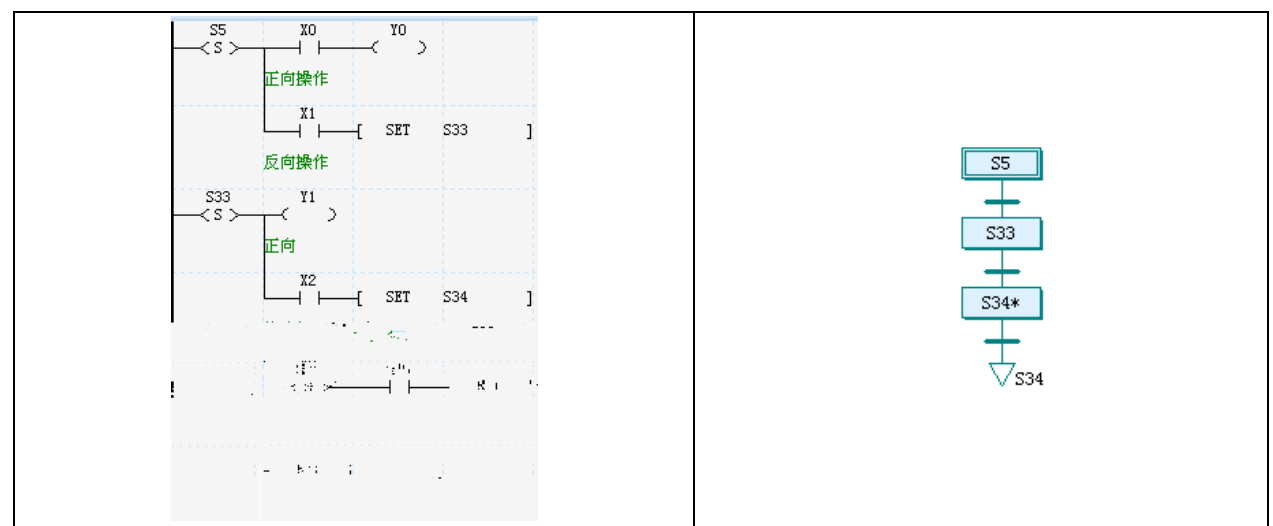
STL ON OFF

5.3.1 STL SFC

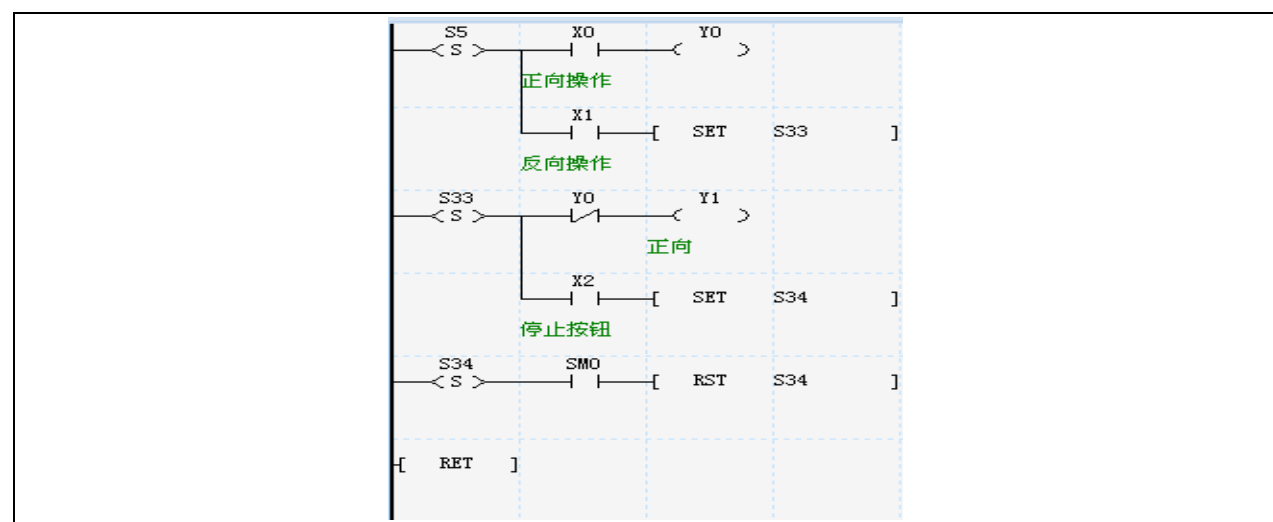
S20 T2 S0 S20 T2 S21 S22

SFC

				Y0	Y1		X0		X1	
X2		Y0	Y1			ON			X1	S5
	S33		Y0	Y1		ON				



Y1 Y0

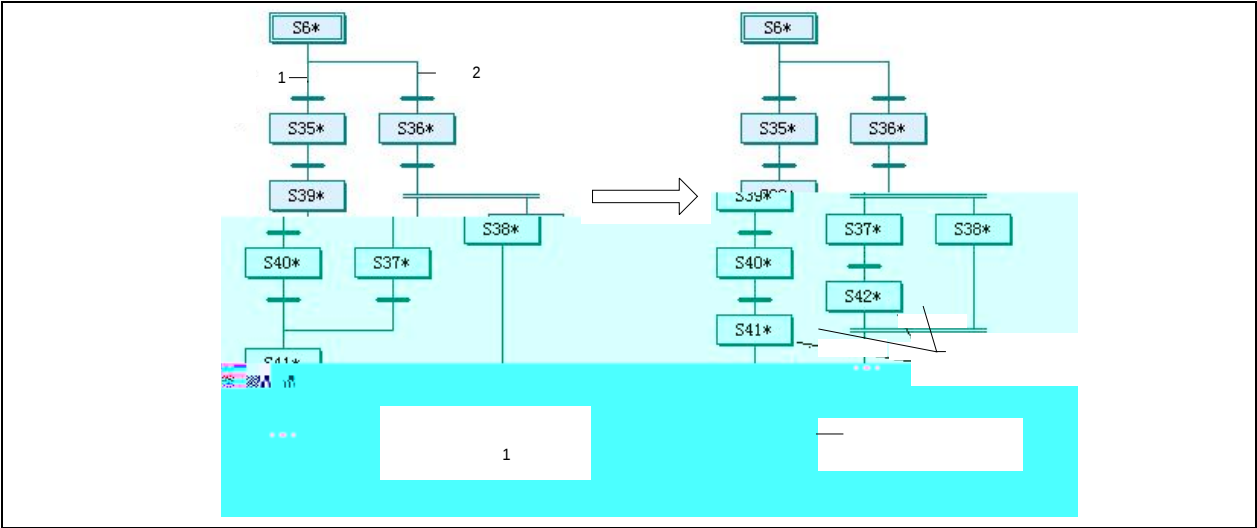


10.

OUT SET SET OUT

11.

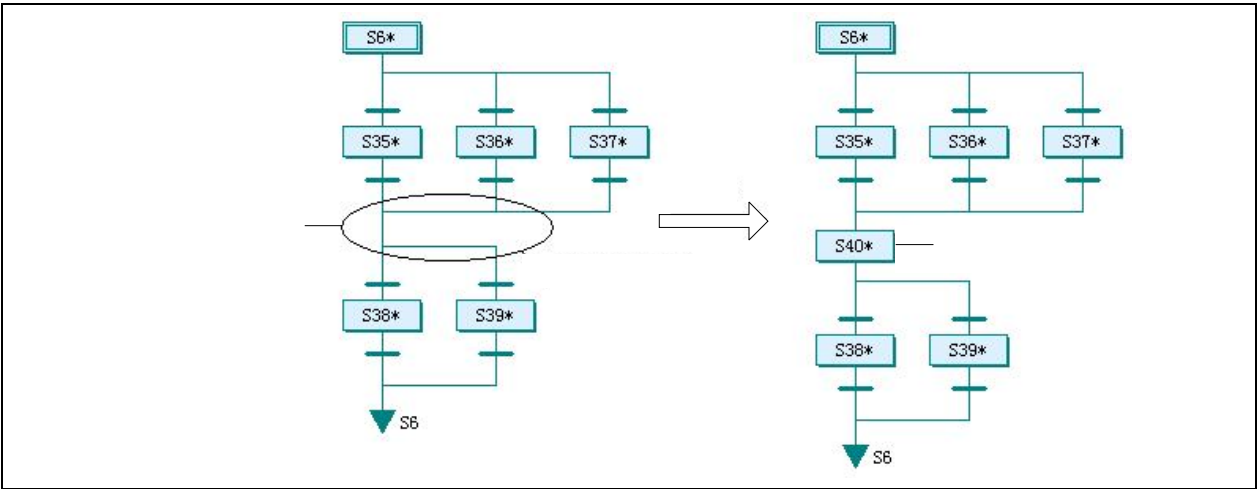
1 S41 2

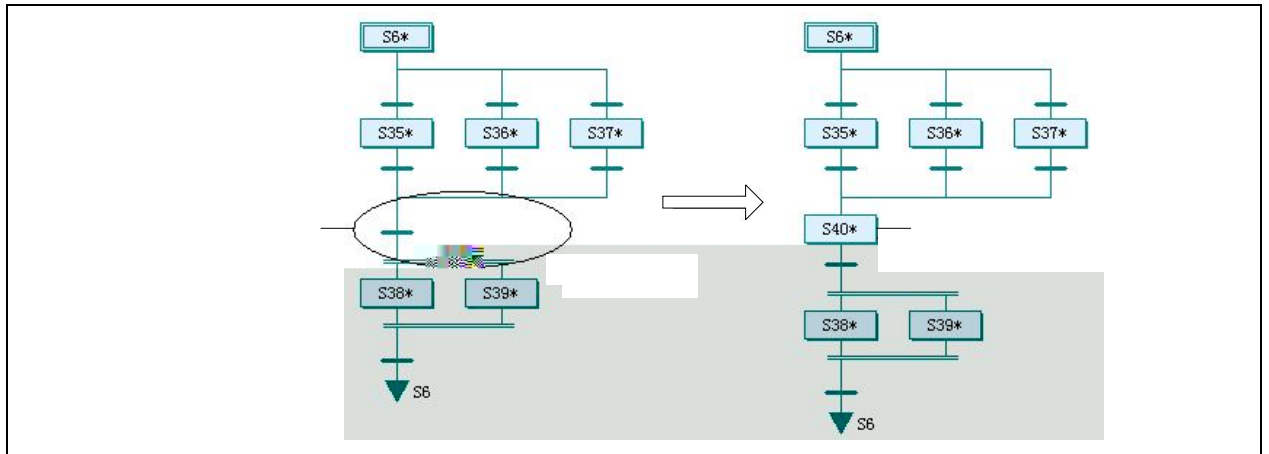


S38 S41 S43 S42 S41 S43 S41

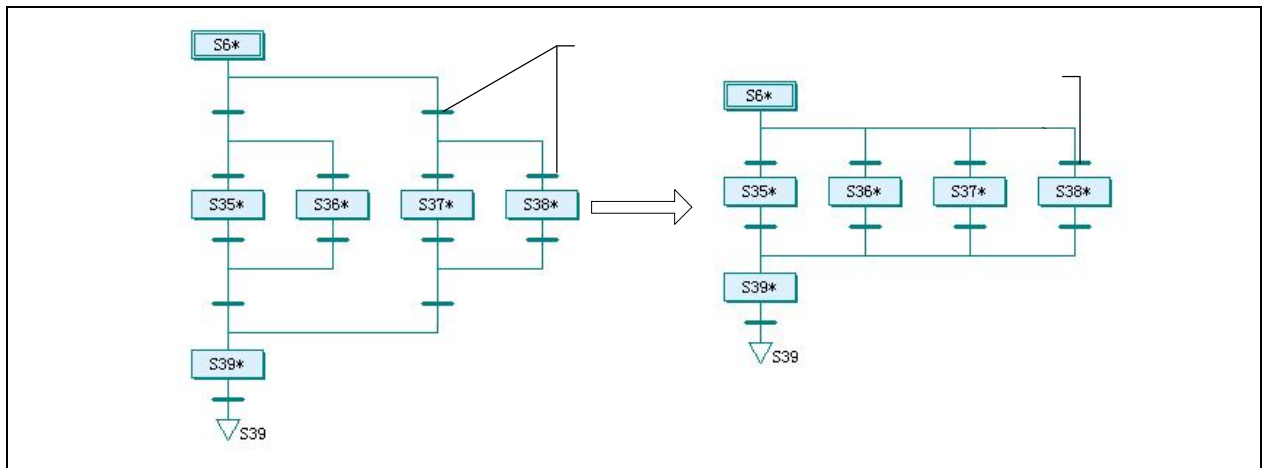
7.4.2

1.





2.

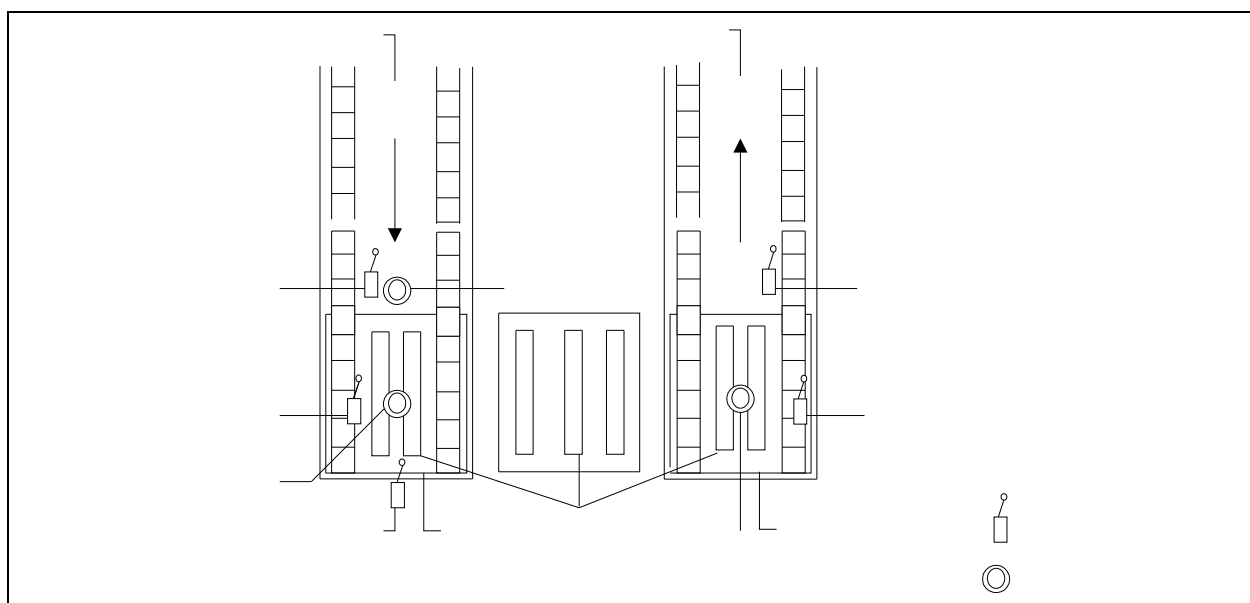


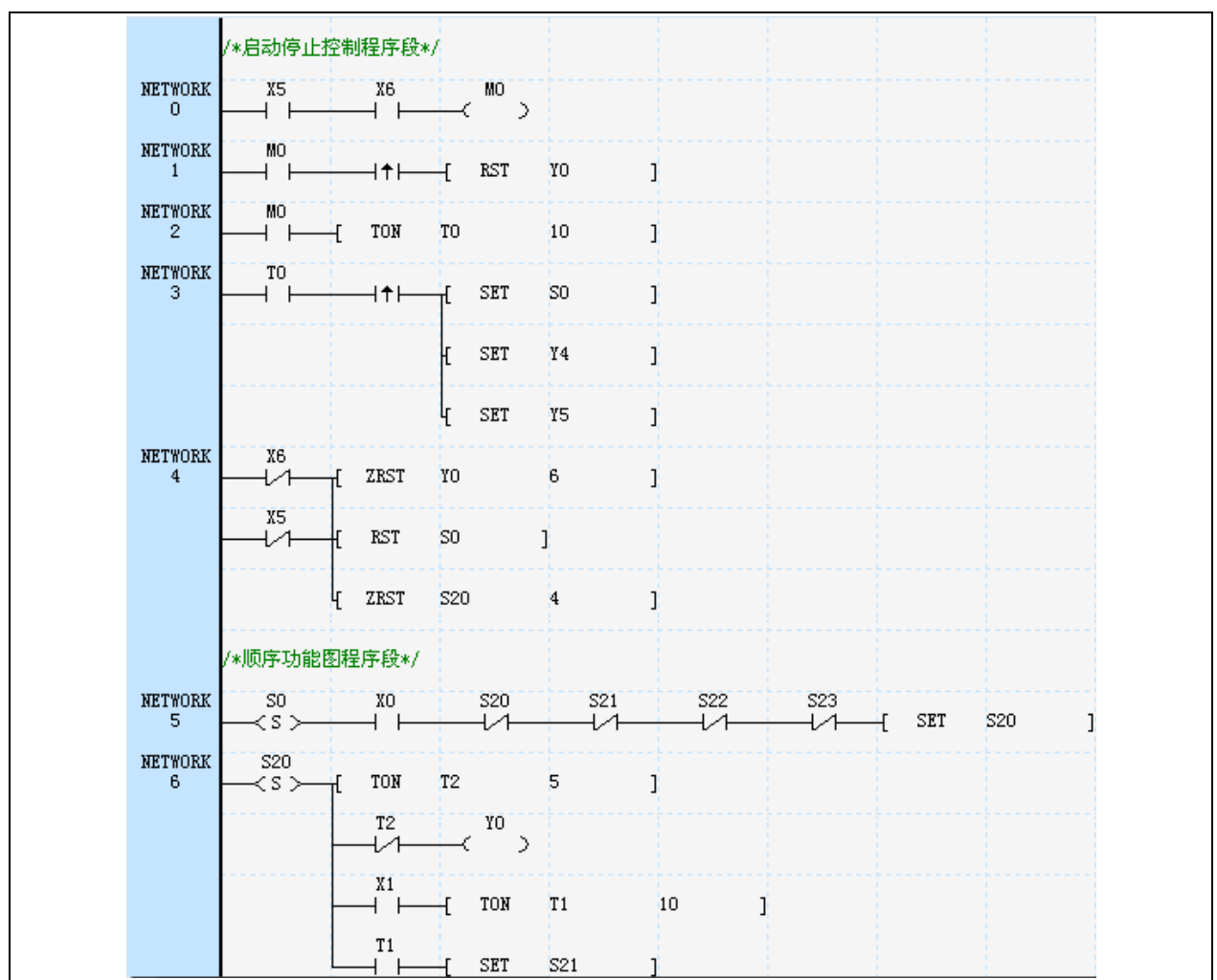
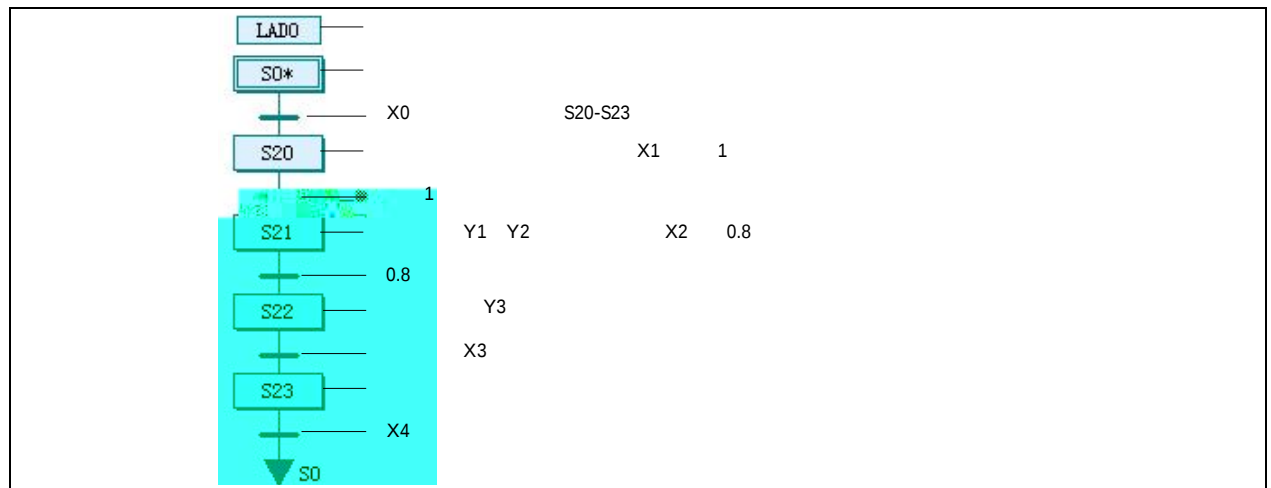
3.

S

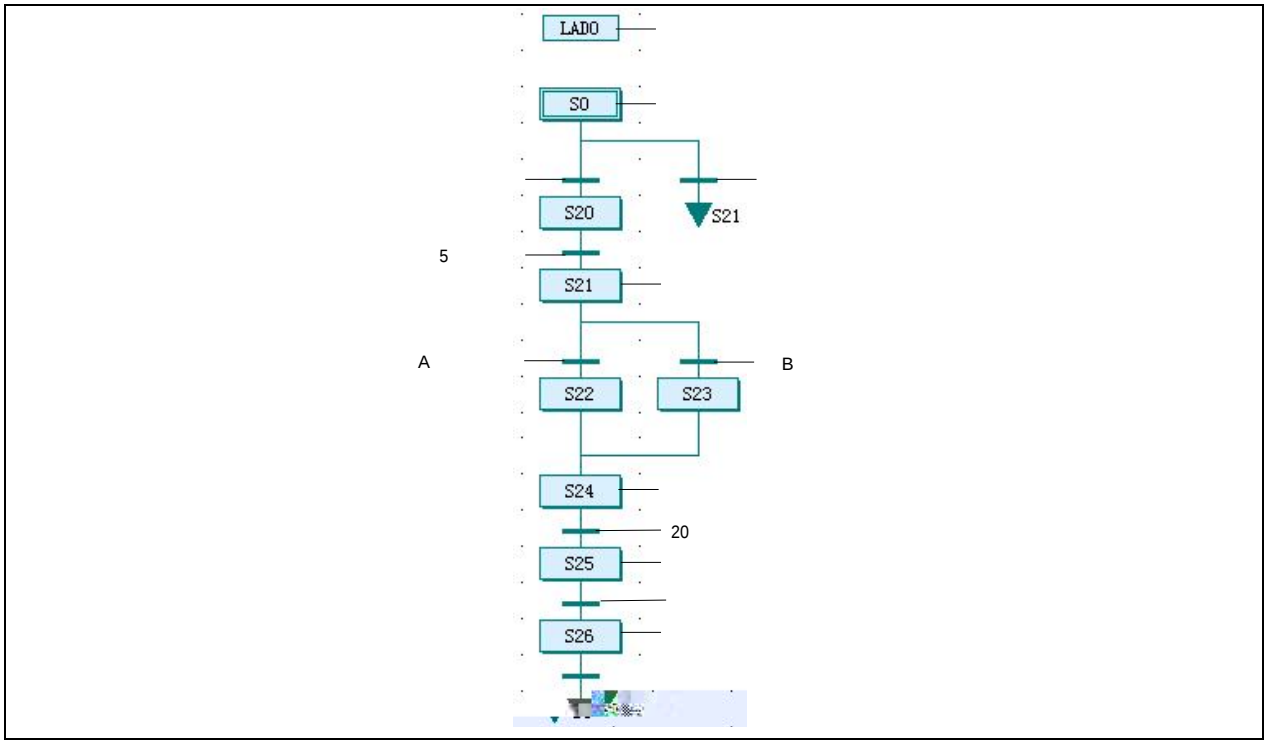
7.5

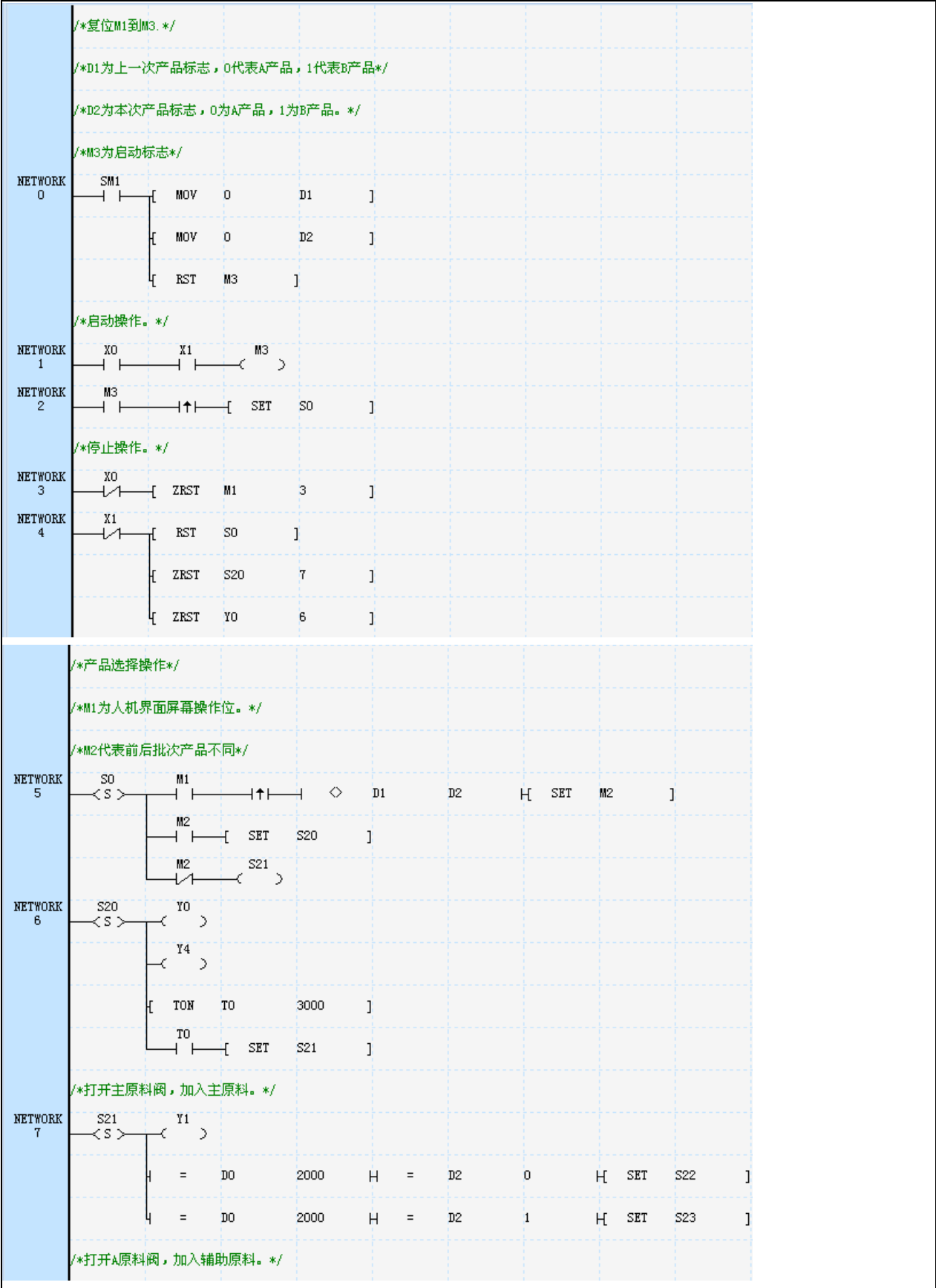
7.5.1

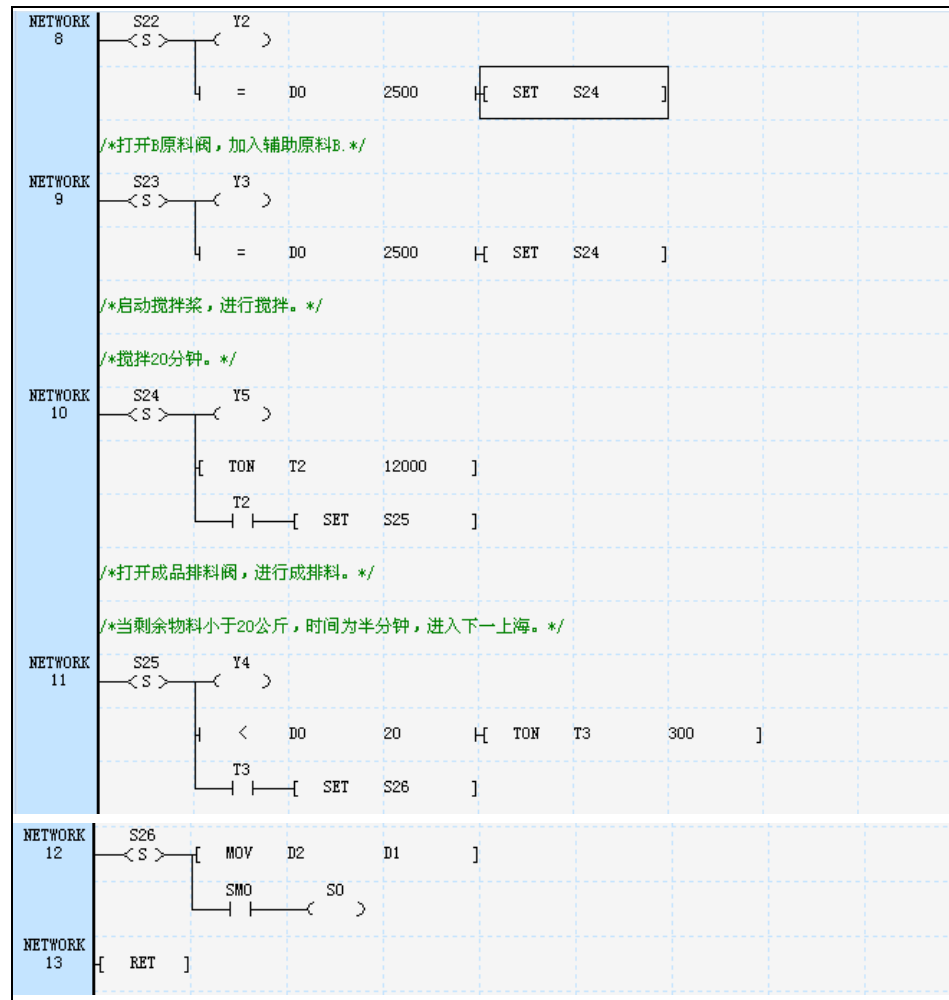




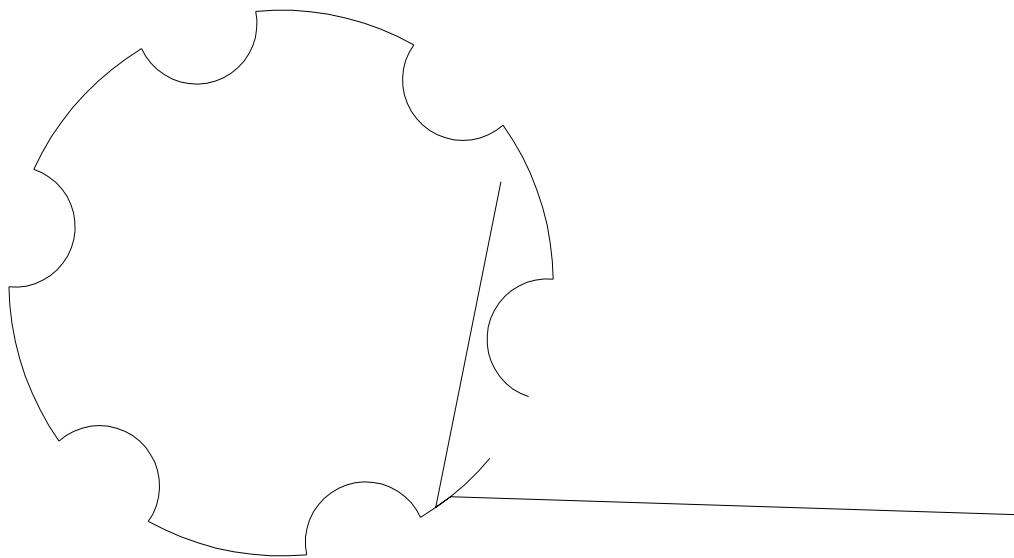
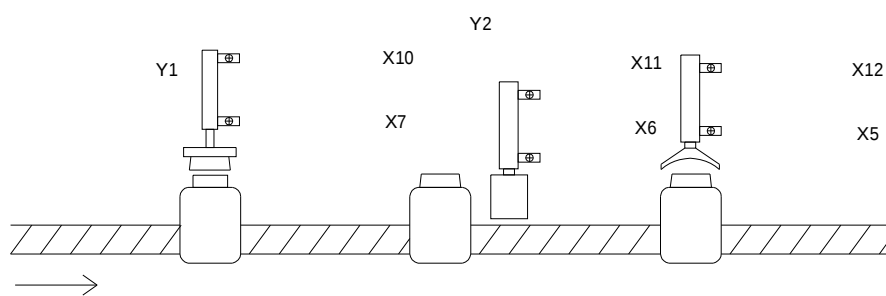
1	X0			10	X11	
2	X1			11	X12	
3	X2			12	Y0	
4	X3			13	Y1	
5	X4	A		14	Y2	A
6	X5	A		15	Y3	B
7	X6	B		16	Y4	
8	X7	B		17	Y5	
9	X10					
A			B			

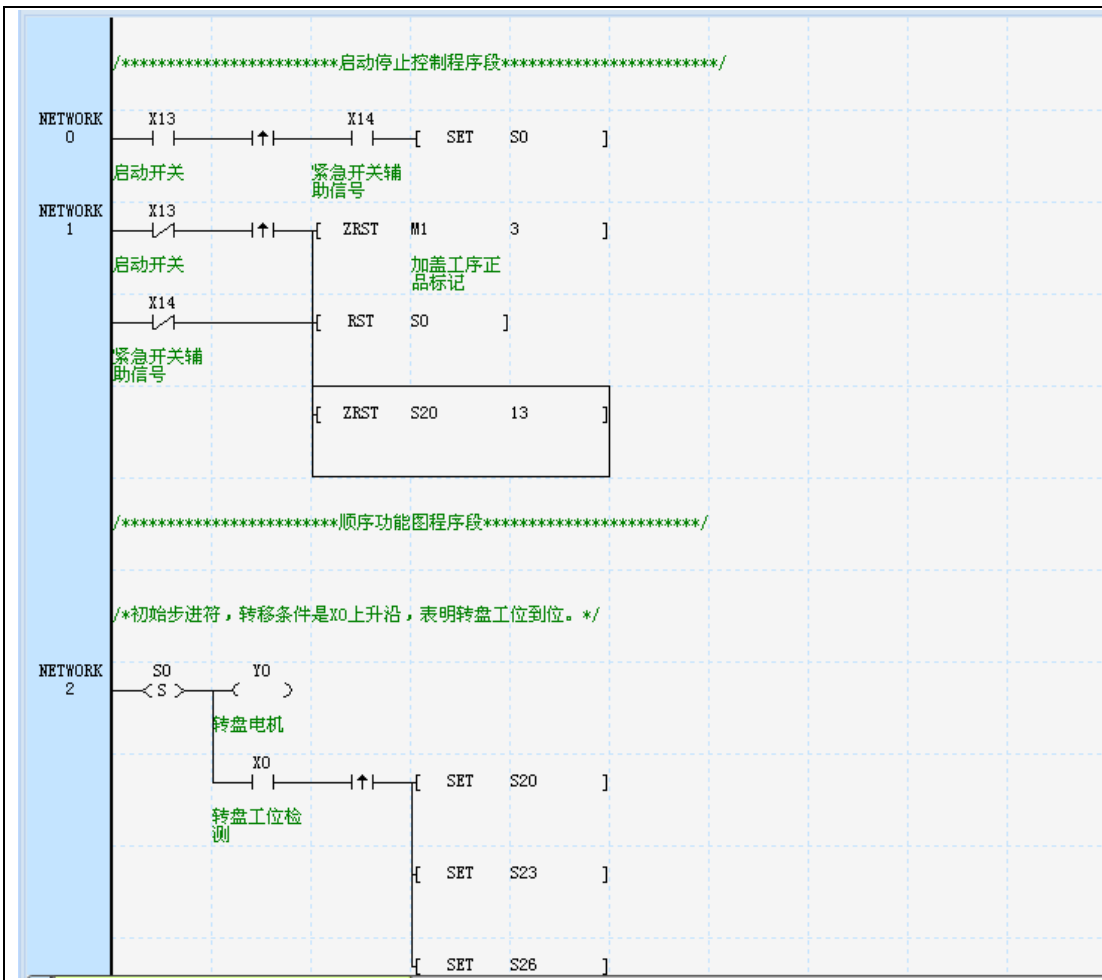
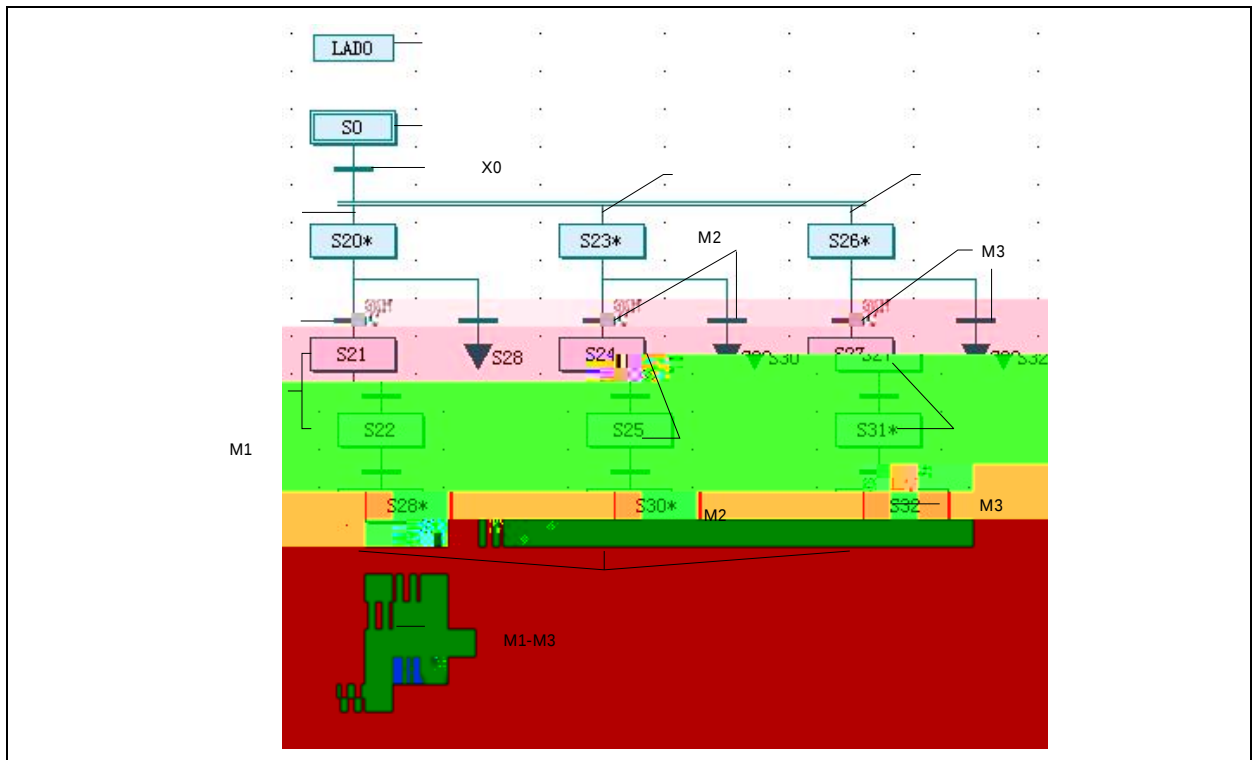


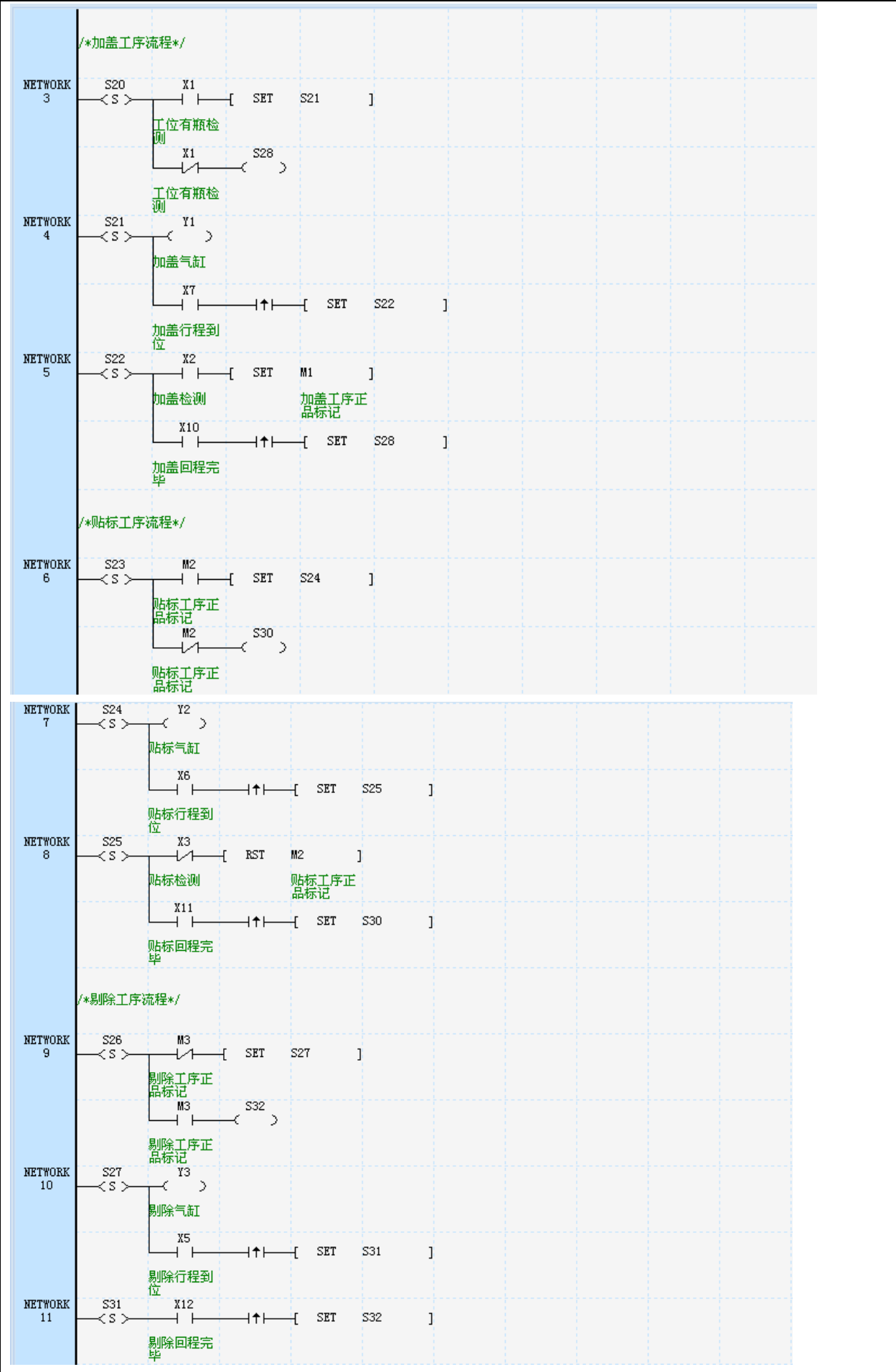


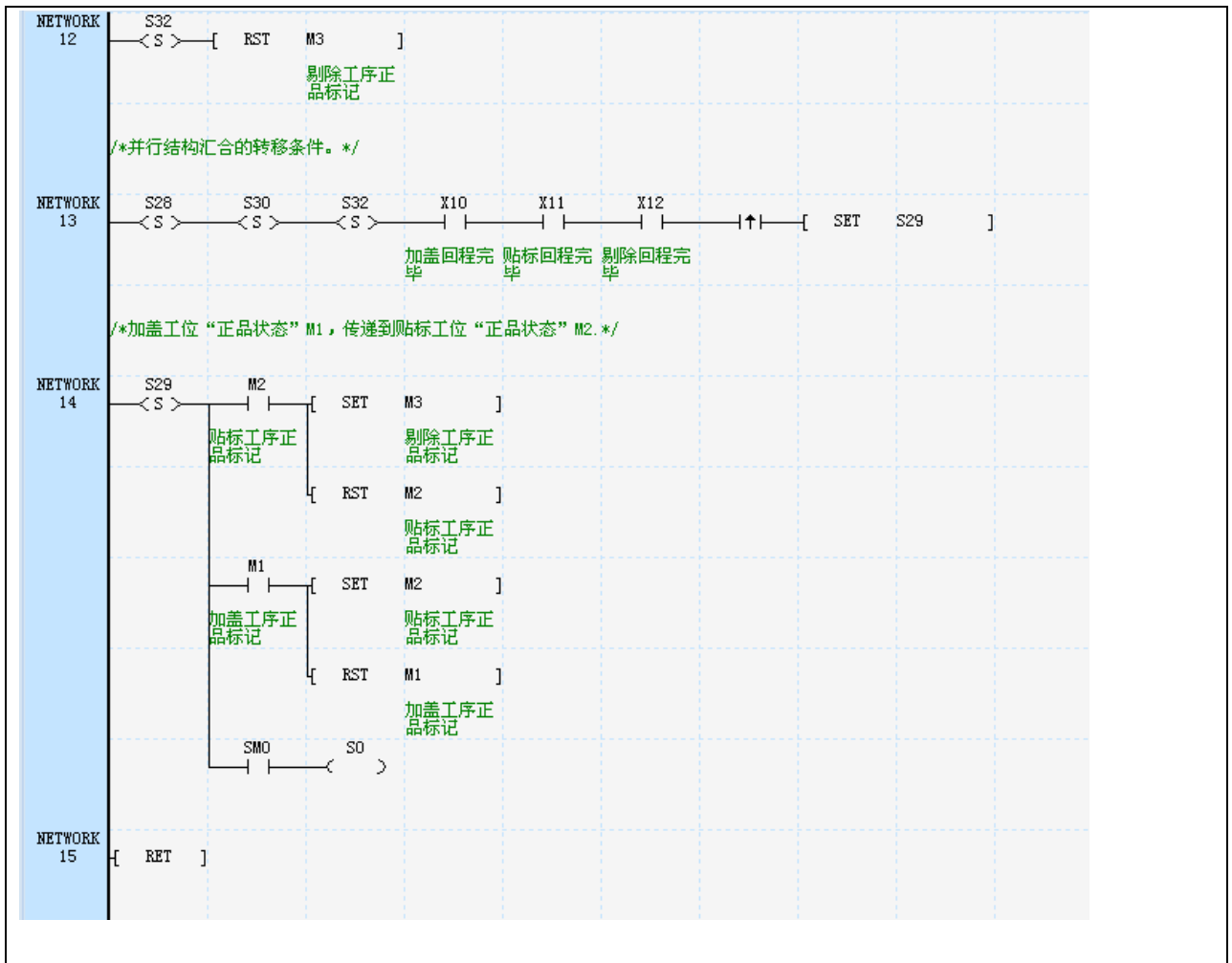


7.5.3









8.1		279
8.1.1		279
8.1.2 MC	PLC	280
8.1.3	SM	280
8.1.4		282
8.1.5 MC200	MC100	285
8.2		285
8.3		286
8.4		286

8.1

8.1.1

MC PLC

		X0	X1	X2	X3	X4	X5	X6	X7	kHz		
										MC280	MC200	MC100
	C236	/								100	50	
	C237		/									
	C238			/								
	C239				/						10	
	C240					/						
	C241						/					
	C301							/				
	C302								/		/	
	C242	/										
	C243				/							
	C244	/									10	
	C245				/							
	C246									100	50	
	C247										10	
	C303										/	
	C248											
	C249										10	
	C250											
	C251	A	B							50	30	
	C304			A	B							
	C305					A	B				/	
	C306							A	B			
	C252	A	B									
	C253				A	B					5	
	C254	A	B									
	C255				A	B						
	C256 (X10)	A	B									
	C257 (X11)			A	B							
	C258 (X12)					A	B					
	C259 (X13)							A	B		/	

PLC

32

/

/

	SM236	SM245	SM301	SM302	ON/OFF	C236	C245	C301	C302	/		
	SM303				C246	C250	C303	/		SM246	SM250	
					SM	OFF		ON				

MC

	C251	SM100
	C252	SM100
	C253	SM102
	C254	SM100
	C255	SM102
	C256	SM100
	C257	SM101
	C258	SM103
	C259	SM104
	C304	SM101
	C305	SM103
	C306	SM104

PLC

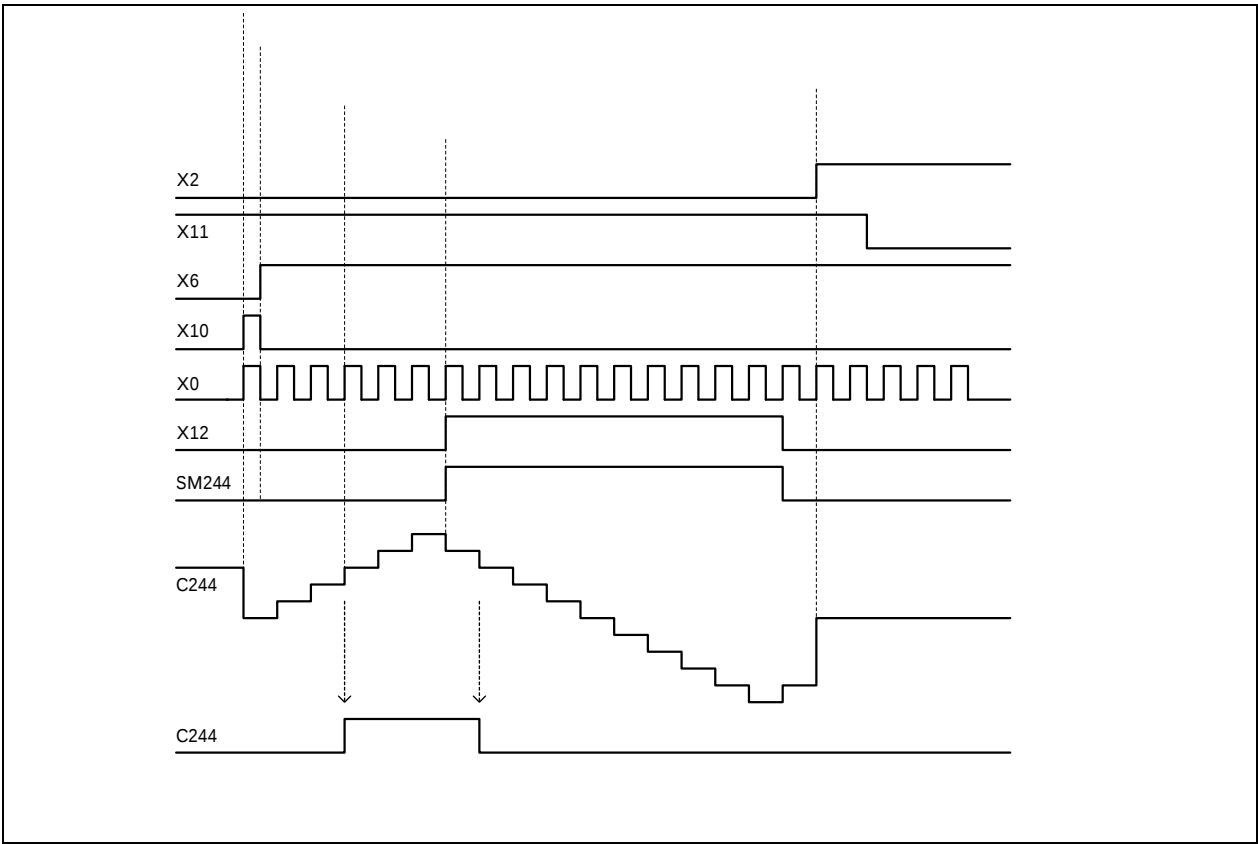
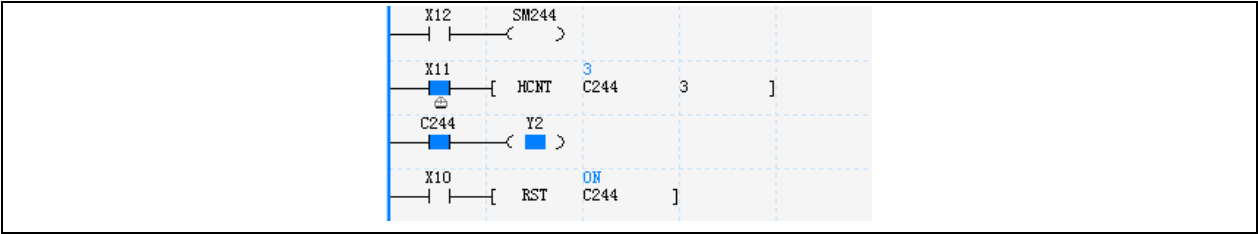
		R/W	MC200	MC100	MC280
SM100	X0 X1 AB 1 /4	R/W	√	√	√
SM101	X2 X3 AB 1 /4	R/W	√	√	√
SM102	X3 X4 AB 1 /4	R/W			√
SM103	X4 X5 AB 1 /4	R/W			√
SM104	X6 X7 AB 1 /4	R/W			√

		/
	C246	SM246
	C247	SM247
	C248	SM248
	C249	SM249
	C250	SM250
	C303	SM303
	C251	SM251
	C252	SM252
	C253	SM253
	C254	SM254
	C255	SM255
	C256	SM256
	C257	SM257
	C258	SM258
	C259	SM259
	C304	SM304
	C305	SM305
	C306	SM306

8.1.4

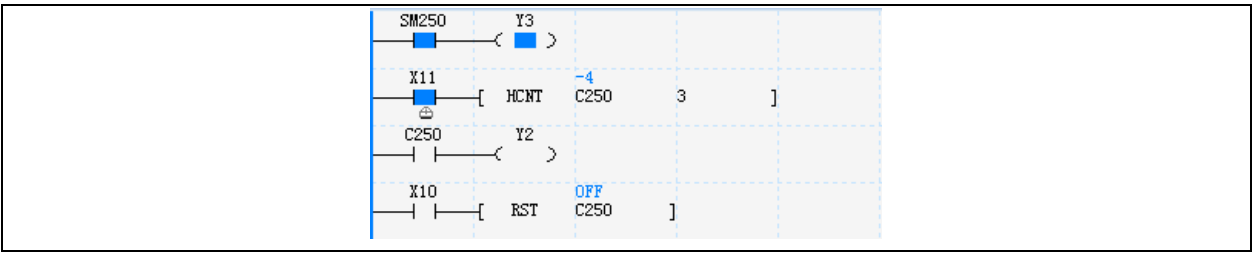
OFF ON

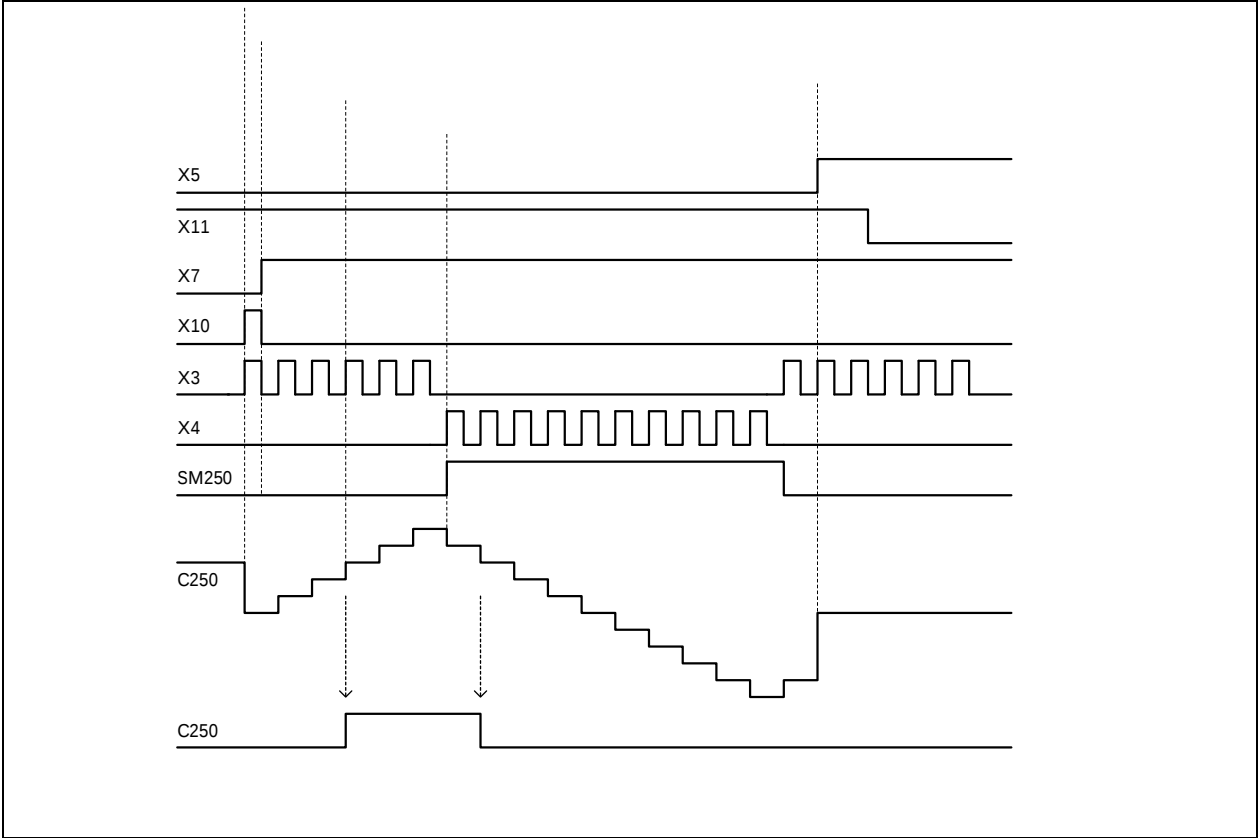
SM



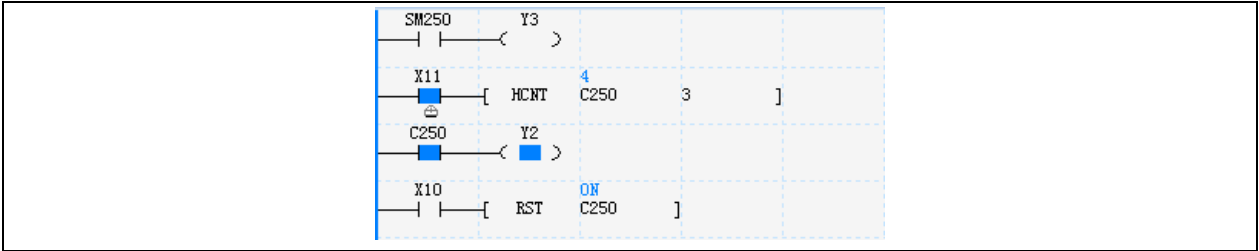
OFF ON

SM





SM OFF ON



8.1.5 MC200 MC100

C236 C237 C246 C251 /

SPD

80kHz(MC100 60kHz)
SPD

DHSCS	DHSCR	DHSCI	DHSZ	DHSP	DHST	80kHz (MC100 60kHz)
DHSCS	DHSCR	DHSCI	DHSP	DHST		30kHz
DHSZ						20kHz

C236 C237 C246 C251

- C236 C237 C246 50kHz
- C251 30kHz

DHSCS DHSCR DHSCI DHSP DHST
10kHz 5kHz
DHSZ 5kHz 4kHz

8.2

X0 X7 SM

		SM
X0		SM90
X1		SM91
X2		SM92
X3		SM93
X4		SM94
X5		SM95
X6		SM96
X7		SM97



- 1 OFF→ON SM ON
- 2 SM90 SM97 HCNT SPD
- 3 PLC
- 4 HCNT SPD
- 5 X0~X7 SPD HCNT 80k
DHSCS DHACI DHSP DHST 30k

8.3

		X0 X7		SPD				PLC	
		1		X0 X7		SPD			
		X0	X7	X0	X7	X0	X7	X0	X7
		X0	X1	X2	X3	X4	X5	X6	X7
C236	C236	/							
	C237		/						
	C238			/					
	C239				/				
	C240								
	C241					/			
	C301						/		
	C302								
	C242	/							
	C243				/				
	C244	/							
	C245								
	C246								
	C247								
	C303								
C248	C248								
	C249								
	C250								
	C251	A	B						
	C304			A	B				
C205	C205								
	C206								

SM16		0.1ms 16	R/W	
SD16		0-20971 0.1ms ,16 SM16 0.1m 20971	R/W	0-20971

SD16

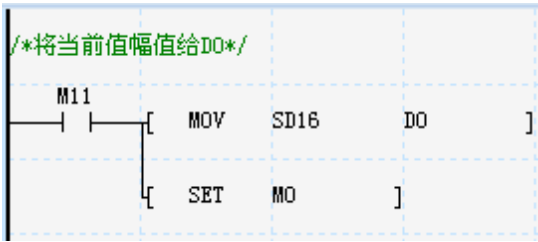
D200 X0 X1 X0 X1
0.1ms



X0



X1



9.1			288
9.2			289
9.3			289
9.4			291
9.5			292
9.6	PTO		294
9.7			294
9.8			295

9.1



9.2

1
8
2
(1)
(2)

(3)

(4)
(5)
3

4 8



1
2
3 I/O REF REF I/O
4 SM SM ON /
5

9.3

SD ms
4ms
SM ON/OFF / OFF
MC PLC 3

9-1

		SD	SM
0	26	SD66	SM66
1	27	SD67	SM67
2	28	SD68	SM68

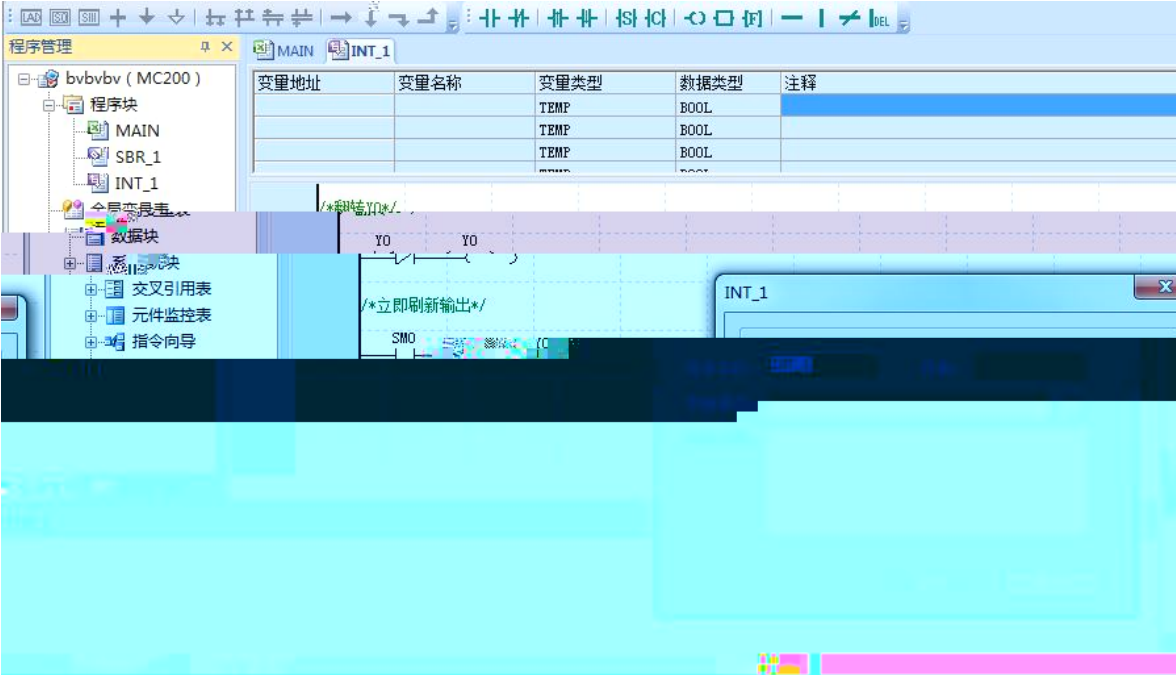


1
2

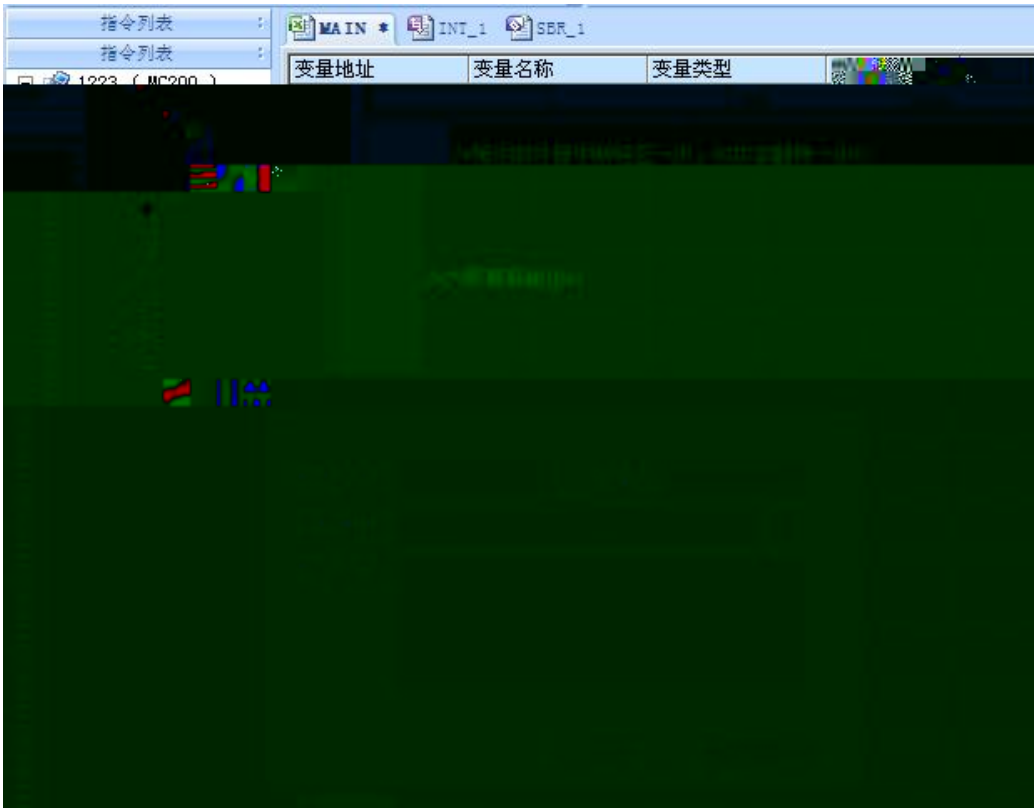
0 Y0 Y0



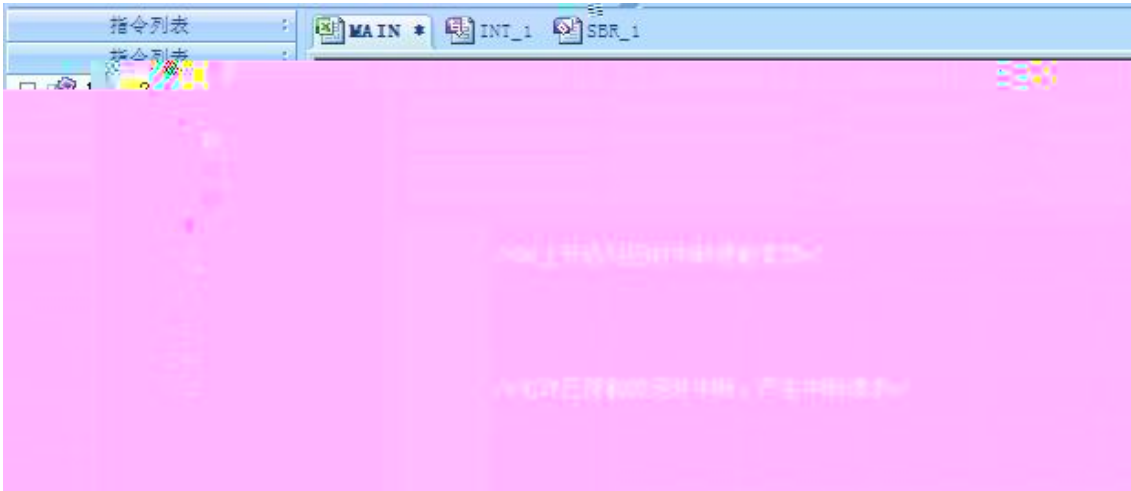
2



1 X0 0 X0 Y0
 Y0



2 EI X0 SM40



9.5

 HCNT DHSCI 20 25
EI

X0

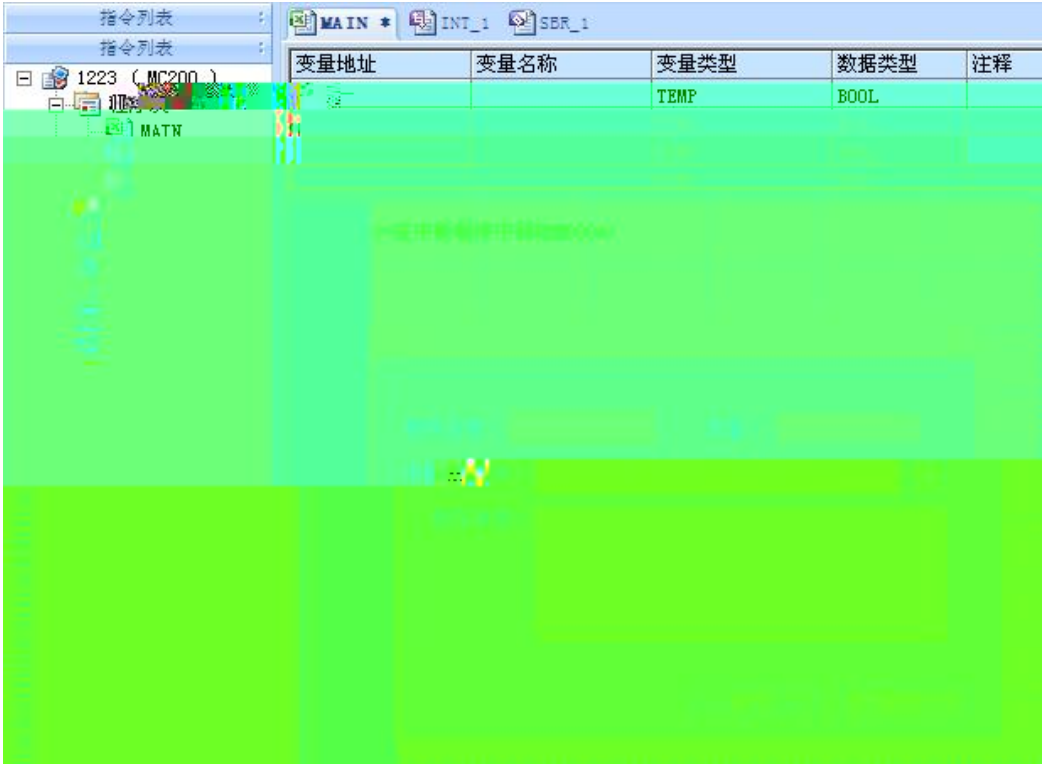
C236

DHSCI

20

1

INT_1

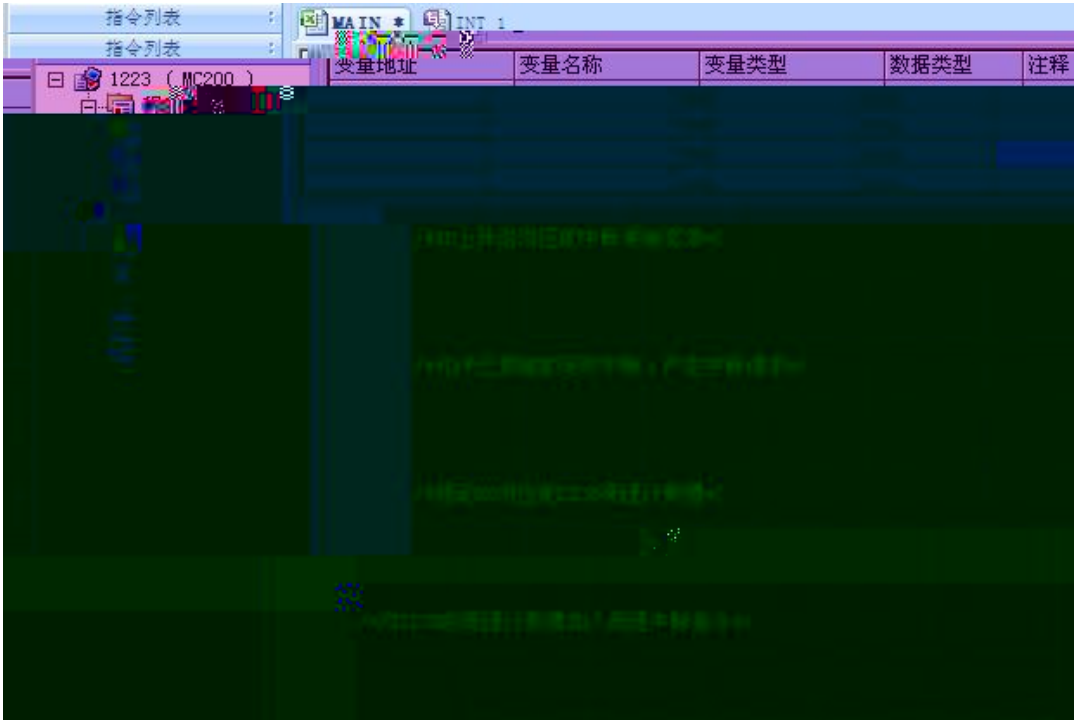


2

EI

SM65

C236



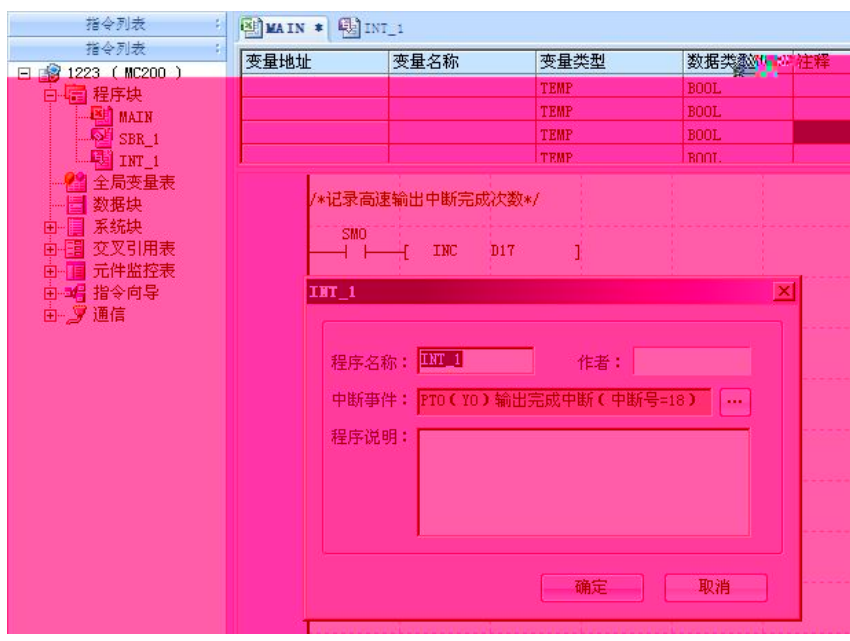
9.6 PTO

PTO

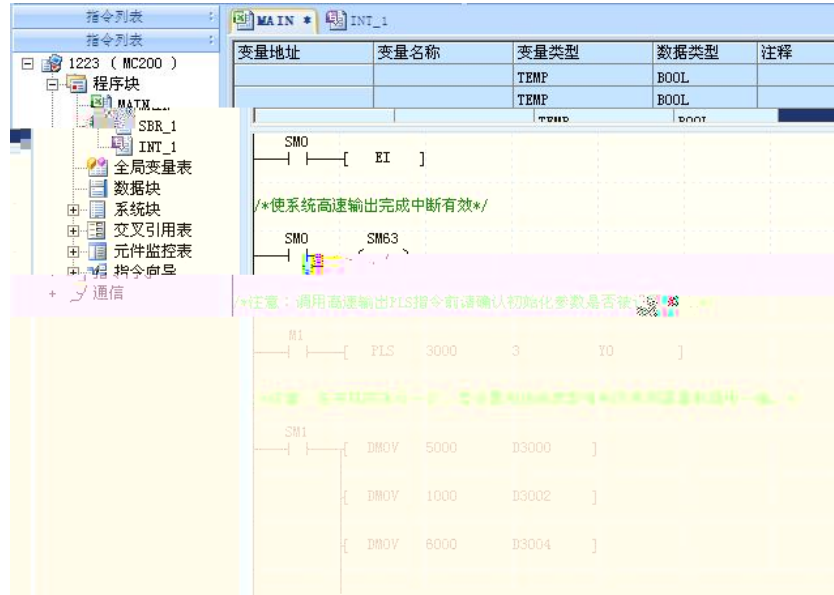
SM63 SM64 Y0 Y1 PTO
MC100

PTO

Y0 Y0 18
INT_1
INT_1



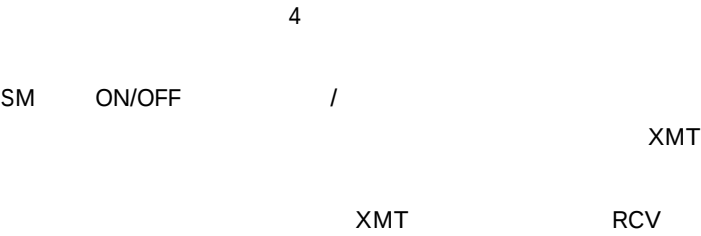
2 MAIN PTO SM63 PLS



9.7

SM56
MC100

9.8



		SM
30	0	SM48
31	0	SM49
32	0	SM50
33	0	SM51
34	1	SM52
35	1	SM53
36	1	SM54
37	1	SM55
8	2	SM59
9	2	SM60
38	2	SM57
39	2	SM58



3



	MC	PLC	
10.1			299
10.2			299
10.3			299
10.3.1			299
10.3.2			299
10.3.3			300
10.3.4			302
10.3.5			302
10.3.6 RTU			302
10.3.7 ASCII			303
10.3.8 Modbus			303
10.3.9 PLC			303
10.3.10 Modbus			304
10.3.11			304
10.3.12			305
10.3.13 LONG INT			305
10.3.14			305
10.3.15			306
10.3.16 Modbus			306
10.3.17 Modbus			307
10.3.18			309
10.4 MCbus			312
10.4.1 MCbus			312
10.4.2 MCBUS			312
10.4.3 MCbus			312
10.4.4 MCbus			314
10.4.5			318
10.4.6 MCbus			319
10.5			320
10.5.1			320
10.5.2			320
10.5.3 M N			320
10.5.4 MCbus			320

10.1

MC		PLC	
Modbus		115200	57600 38400 19200 9600 4800 2400 1200
MCbus		115200	57600 38400 19200 9600 4800 2400 1200

MC		PLC	
MC200	0	RS232	Modbus MCbus
	1	RS232 RS485	Modbus MCbus
MC100	0	RS232	Modbus MCbus
	1	RS232 RS485	Modbus MCbus
MC280	0	RS232	Modbus MCbus
	1	RS485	Modbus MCbus
	2	RS485	Modbus MCbus

MC PLC RUN STOP TM 0

10.2

X_Builder

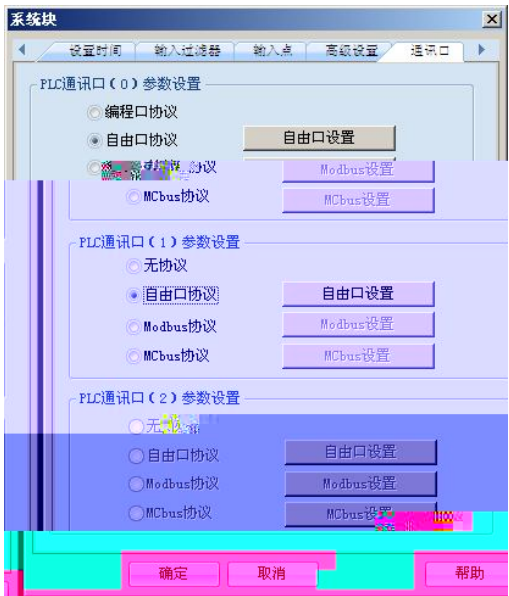
10.3

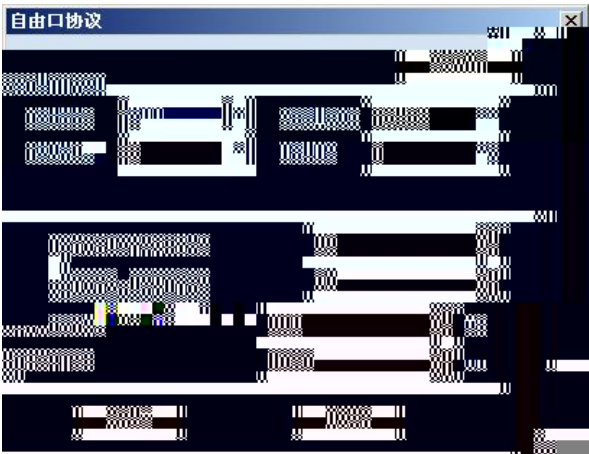
10.3.1

ASCII

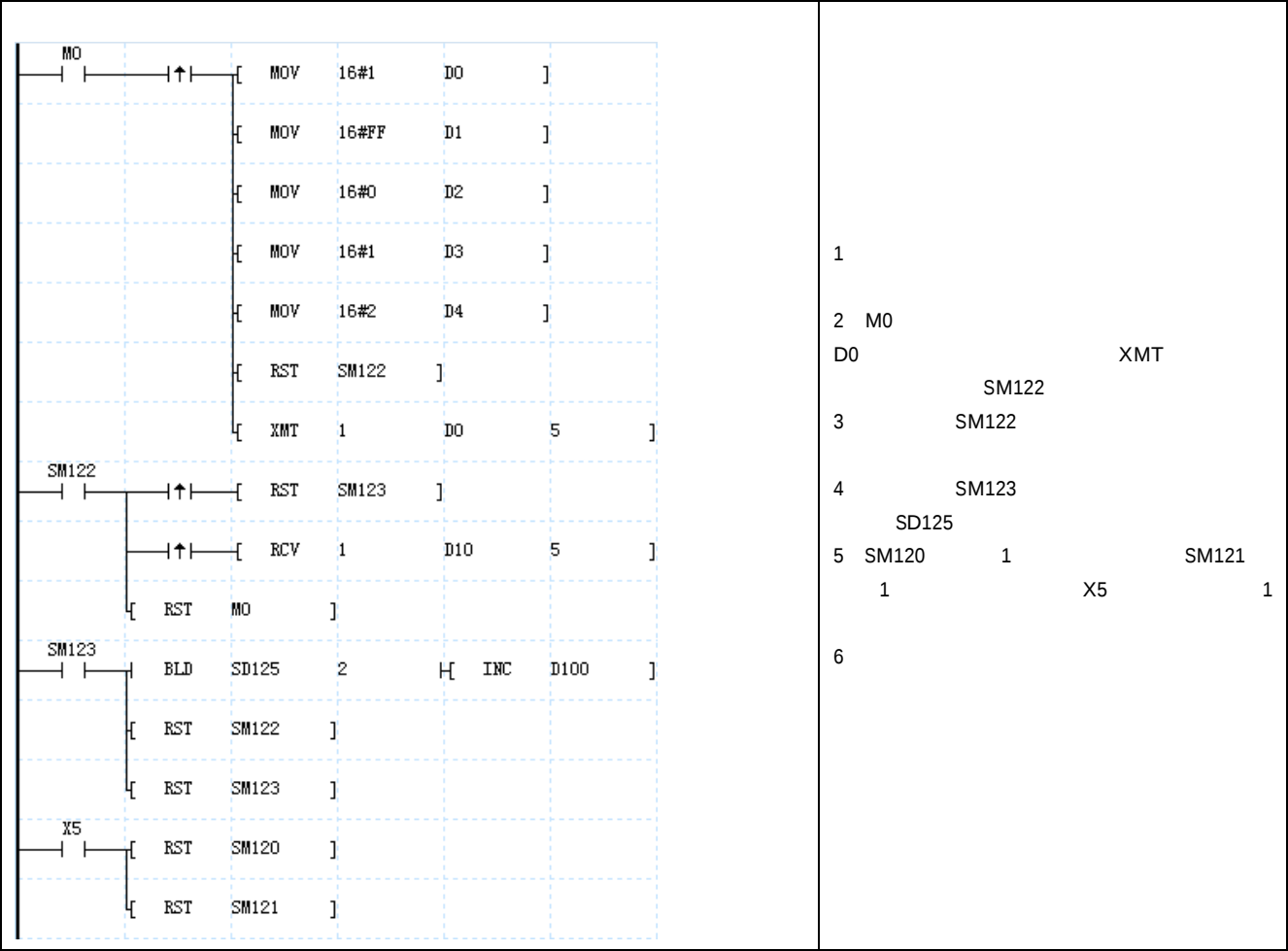
PLC RUN
XMT RCV

10.3.2



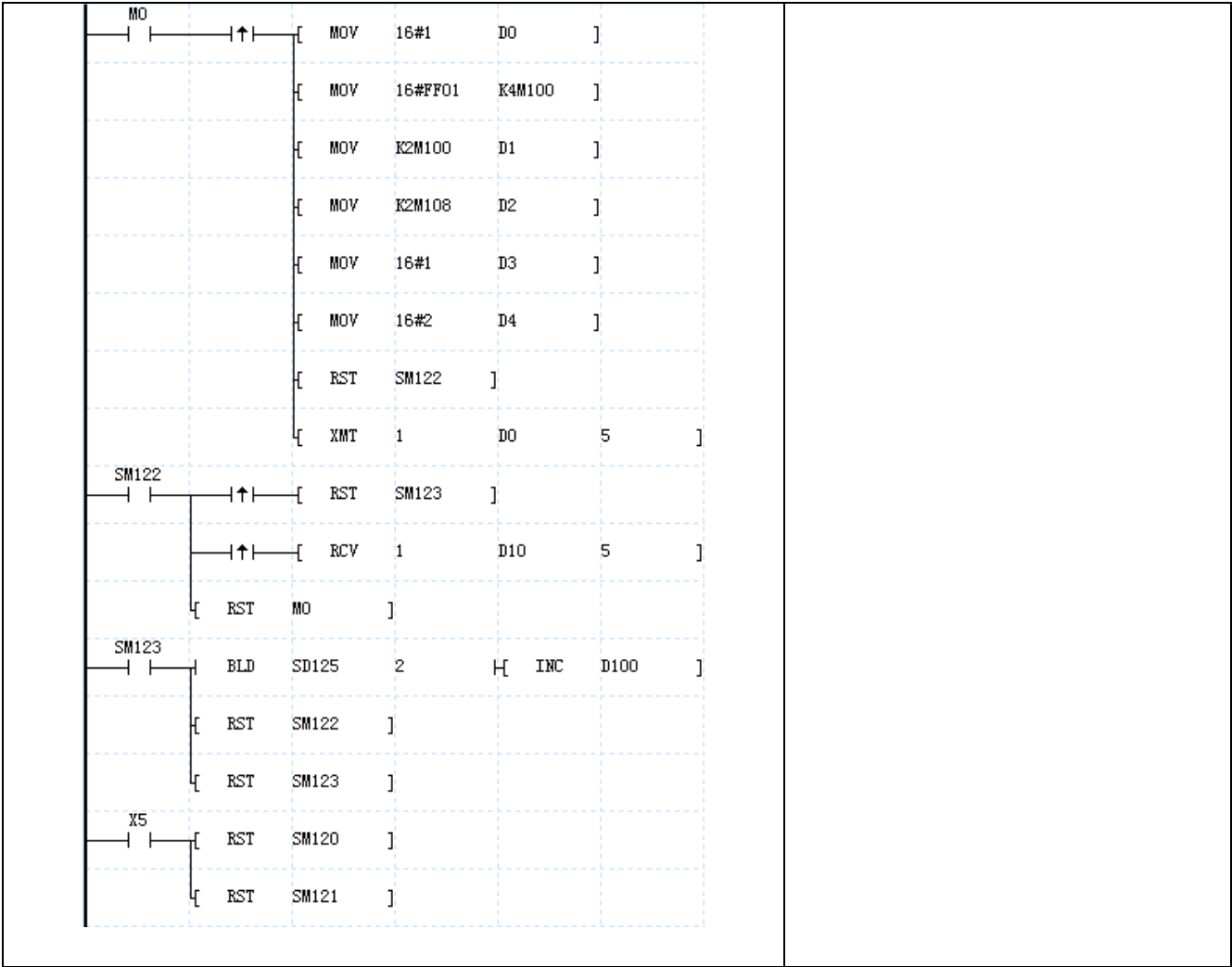


	115200 57600 38400 19200 9600 4800 2400 1200 9600	
	7 8 8	
	1 2 1	
	0 255 00 FF	
	0 255 00 FF	
	0 65535ms	



2 1





10.3.4

MC PLCModbus ASCII RTU MC100 RTU

10.3.5

1 RS232 RS485
2
 (1) 7 ASCII 8 RTU
 (2) 1200 2400 4800 9600 19200 38400
 (3)
 (4) 1 2
3 31 1 31

10.3.6 RTU

1
2 1.5
3 3.5

4 CRC16

5 RTU 256

				CRC
	1	1	0 252	2

6

19200 1.5 =1/19200 11 1.5 1000=0.86ms
 3.5 =1/19200 11 3.5 1000=2ms

10.3.7 ASCII

1 ASCII

2 3A CRLF 0D 0A

3 1s

4 LRC

5 ASCII RTU ASCII HEX ASCII 2 252
 RTU 252 ASCII 513

					LRC	
	1	2	2	0 2*252	2	2

10.3.8 Modbus

Modbus 01 02 03 04 05 06 15 16 41
 41

10.3.9 PLC

		Modicon		
01		0 ¹ :xxxx	Y X M SM S T C	
02		1 ² :xxxx	X	
03		4 ³ :xxxx ⁴	D SD Z T C	
05		0:xxxx	Y M SM S T C	
06		4:xxxx	D SD Z T C	
15		0:xxxx	Y M SM S T C	
16		4:xxxx	D SD Z T C	
1 0 2 1 3 4 4 xxxx 1 9999 1 9999 0 5 0 1 4 6 05 15 X X				

2 PLC Modbus

Y		Y0 Y377 8 256	0000 0255	01 05 15	Y0 Y7
X		X0 X377 8 256	1200 01455		Y10 Y17

000 01 01 257 Y
01 83 3 00 51
257(è)0250™0256p1 #< Y
3 01 01 0 00 A0 7D AD
100 00 A0 160
01 83 2 C1 1
100 Y 156 160
01 8 01 0
p1 ! @ 0250™0256p1 #< Y
1 X X SM SD
2 01 CRC

10.3.12

C C200 2C255 C200 C255
03 16 tœC T\$,C)1ò/™™™™€ & r p1 s+ @ •

08	00			08	12	
08	01			08	13	
08	04			08	14	
08	10			08	15	
08	11			08	18	

MC200/MC280

10.3.15

0x01	
0x02	
0x03	

- (1)
- (2)RTU256
- (3)RTU
- (4)
- (5)ASCII



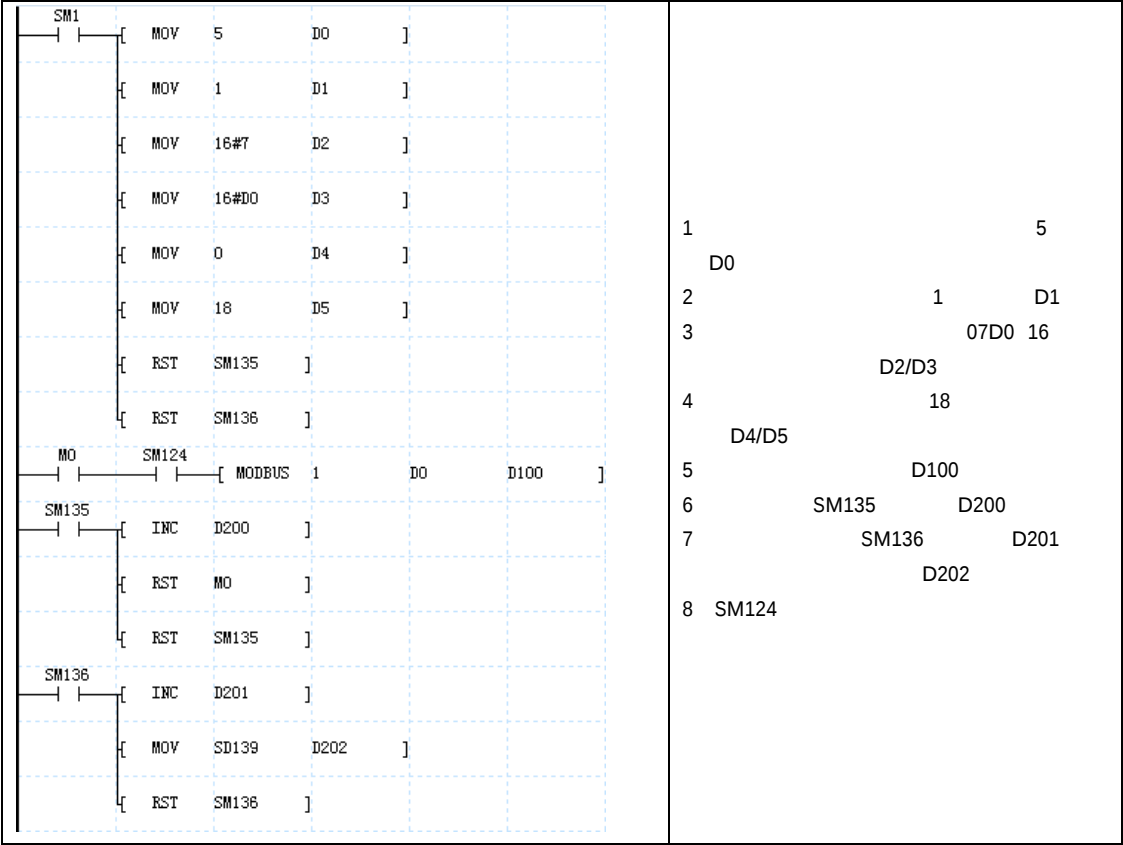
10.3.16 Modbus

	PORT0	PORT0	PORT1	PORT0	Modbus	PORT1	Modbus
Modbus							
Modbus				Modbus			
	031						
	1152005760038400192009600480024001200						
	78ASCII7RTU8						
	1212						
Modbus /	10						
	RTUASCII						



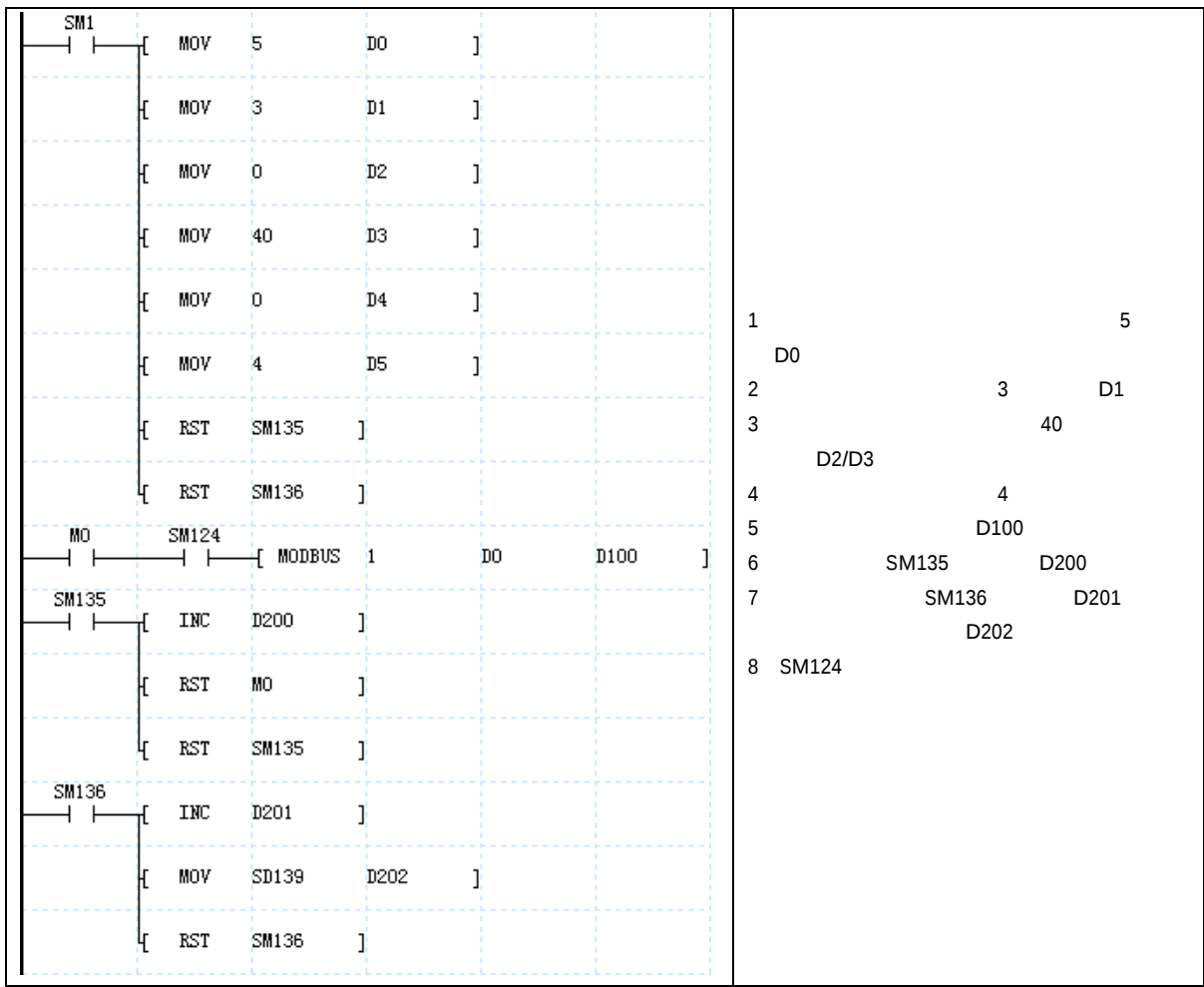
1	MC200 PLC	1	0	11
39		12		
2			Modbus	
		Modbus		
SD139	D202	D202		
3			MC200	Modbus
	MC200	PLC		

2	MC200	Modbus	MC200	5	2000	2017		
			D100	D100	D101	D102		D103



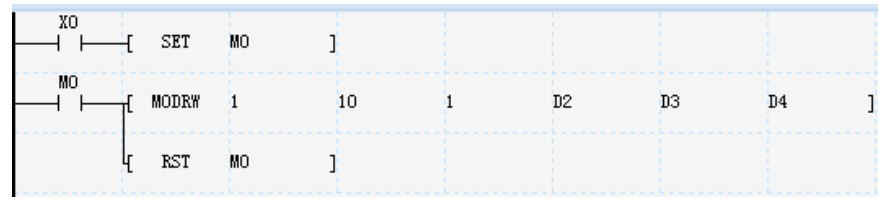
3 MC200 Modbus MC200 5 40 43
D100 D100 D101 D102 D103

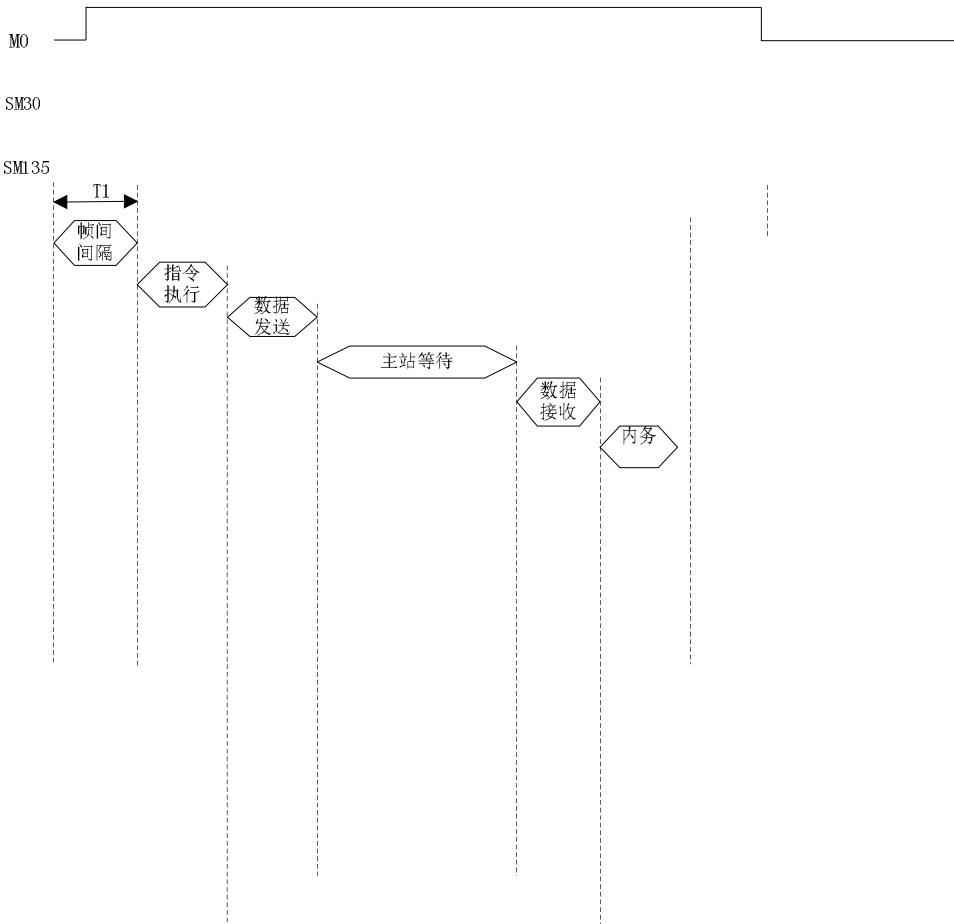
40 8	40 8	41 8	41 8	42 8	42 8	43 8	43 8
D103	D104	D105	D106	D107	D108	D109	D110



10.3.18

MODBUS





T_{12}

1ms

1920081RTU1020

T_5

$\frac{10}{19200}$

10001

6.2ms

T_7

$\frac{20}{19200}$

10001

11.4ms

T_4

T_8

T_9

1ms

T_6

35ms

T_3

16.23511.411

55.6ms

10ms

T_2

$(INT(\frac{55.6}{15})+1)15$

60ms

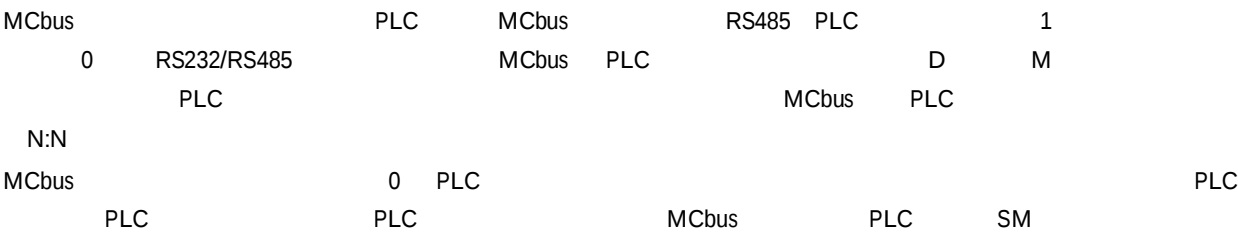
T_{10}

6.215111.4

33.6ms

10.4 MCbus

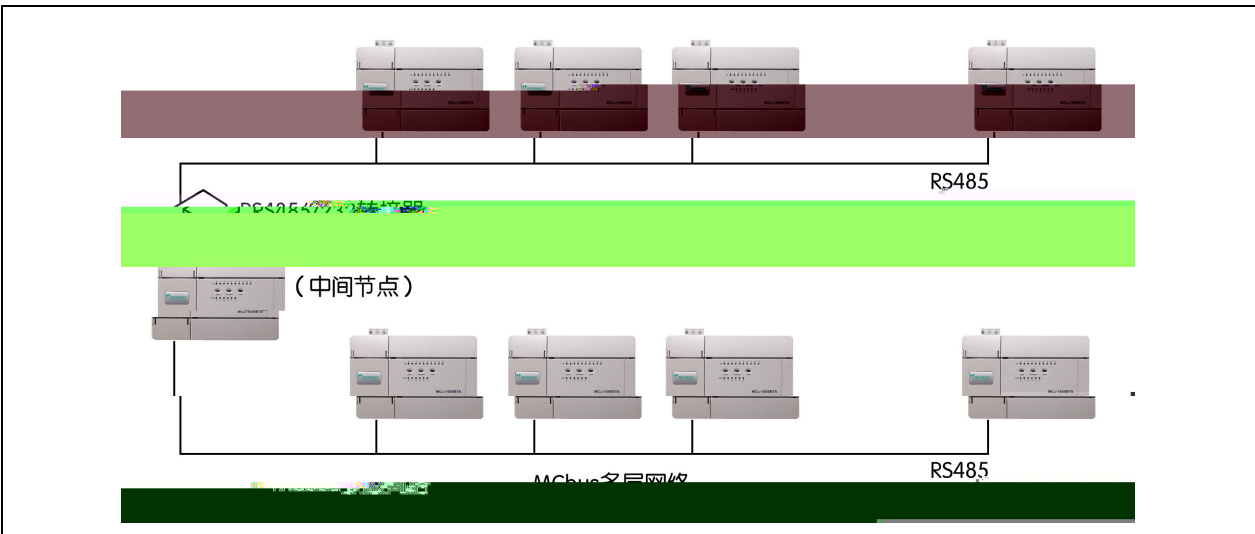
10.4.1 MCbus



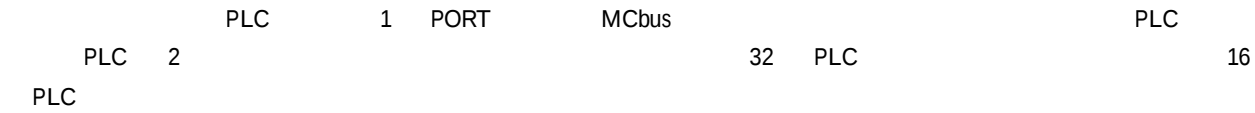
10.4.2 MCbus



10-1 MCbus



10-2 MCbus



10.4.3 MCBUS



10-1

10-5

1

0

1



(1#)



1#



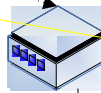
(2#)

1#



(3#)

1#



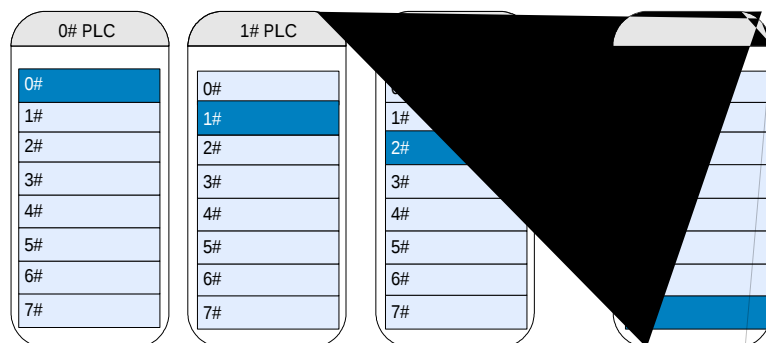
(N#)

RS 485

RS 485

10-3

MC



3	4	5
#7		

D7701 0# PLC D7700 D7701 1#-
D7703 0# PLC D7700 D7701 D7702 D7703

3	4	5
#0	#0	#0
#1		
#2	#1	#0
#3		

#4
#2
#1

MCbus D 0

D	6	7	8	9
D7700 D7701	#0	#0	#0	#0
D7702 D7703	#1			
D7704 D7705	#2			
D7706 D7707	#3	#1	#1	
D7708 D7709	#4			
D7710 D7711	#5			
D7712 D7713	#6			
D7714 D7715	#7			
D7716 D7717	#8	#4	#2	#1
D7718 D7719	#9			
D7720 D7721	#10			
D7722 D7723	#11	#5		
D7724 D7725	#12	#6	#3	
D7726 D7727	#13			
D7728 D7729	#14			
D7730 D7731	#15	#7		

6 0# 0 D D7700 D7701 0# PLC D7700 D7701
1#- 15# D7700 D7701

MCbus D 1

D	10	11	12	13
D7732 D7733	#0	#0	#0	#0
D7734 D7735	#1			
D7736 D7737	#2			
D7738 D7739	#3	#1	#1	
D7740 D7741	#4			
D7742 D7743	#5			
D7744 D7745	#6	#3	#2	
D7746 D7747	#7			
D7748 D7749	#8			
D7750 D7751	#9	#5	#2	
D7752 D7753	#10			
D7754 D7755	#11			
D7756 D7757	#12	#6	#3	
D7758 D7759	#13			
D7760 D7761	#14			
D7762 D7763	#15	#7		

10 0# 1 D D7732 D7733 0# PLC D7732 D7733
1#- 15# D7732 D7733

MCbus M 0

M		6	7	8	9
M1400	M1415	#0	#0	#0	#0
M1416	M1431	#1			
M1432	M1447	#2	#1		
M1448	M1463	#3			
M1464	M1479	#4	#2	#1	
M1480	M1495	#5			
M1496	M1511	#6	#3		
M1512	M1527	#7			
M1528	M1543	#8	#4	#2	#1
M1544	M1559	#9			
M1560	M1575	#10	#5		
M1576	M1591	#11			
M1592	M1607	#12	#6	#3	
M1608	M1623	#13			
M1624	M1639	#14	#7		

10.4.5

D	14	15	16	17	18		
D7500 D7507	#0	#0	#0	#0	#0		
D7508 D7515	#1						
D7516 D7523	#2	#1					
D7524 D7531	#3						
D7532 D7539	#4	#1					
D7540 D7547	#5						
D7548 D7555	#6		#3				
D7556 D7563	#7						
D7564 D7571	#8	#4	#2	#1			
D7572 D7579	#9						
D7580 D7587	#10	#5					
D7588 D7595	#11						
D7596 D7603	#12	#6				#3	
D7604 D7611	#13						
D7612 D7619	#14						#7
D7620 D7627	#15						
D7628 D7635	#16	#8	#4	#2			
D7636 D7643	#17						
D7644 D7651	#18	#9					
D7652 D7659	#19						
D7660 D7667	#20	#10	#5				
D7668 D7675	#21						
D7676 D7683	#22	#11					
D7684 D7691	#23						
D7692 D7699	#24	#12	#6	#3			
D7700 D7707	#25						
D7708 D7715	#26	#13					
D7716 D7723	#27						
D7724 D7731	#28	#14	#7				
D7732 D7739	#29						
D7740 D7747	#30	#15					
D7748 D7755	#31						

10.4.6 MCBus

PLC0PLC1MCbus

MCbus



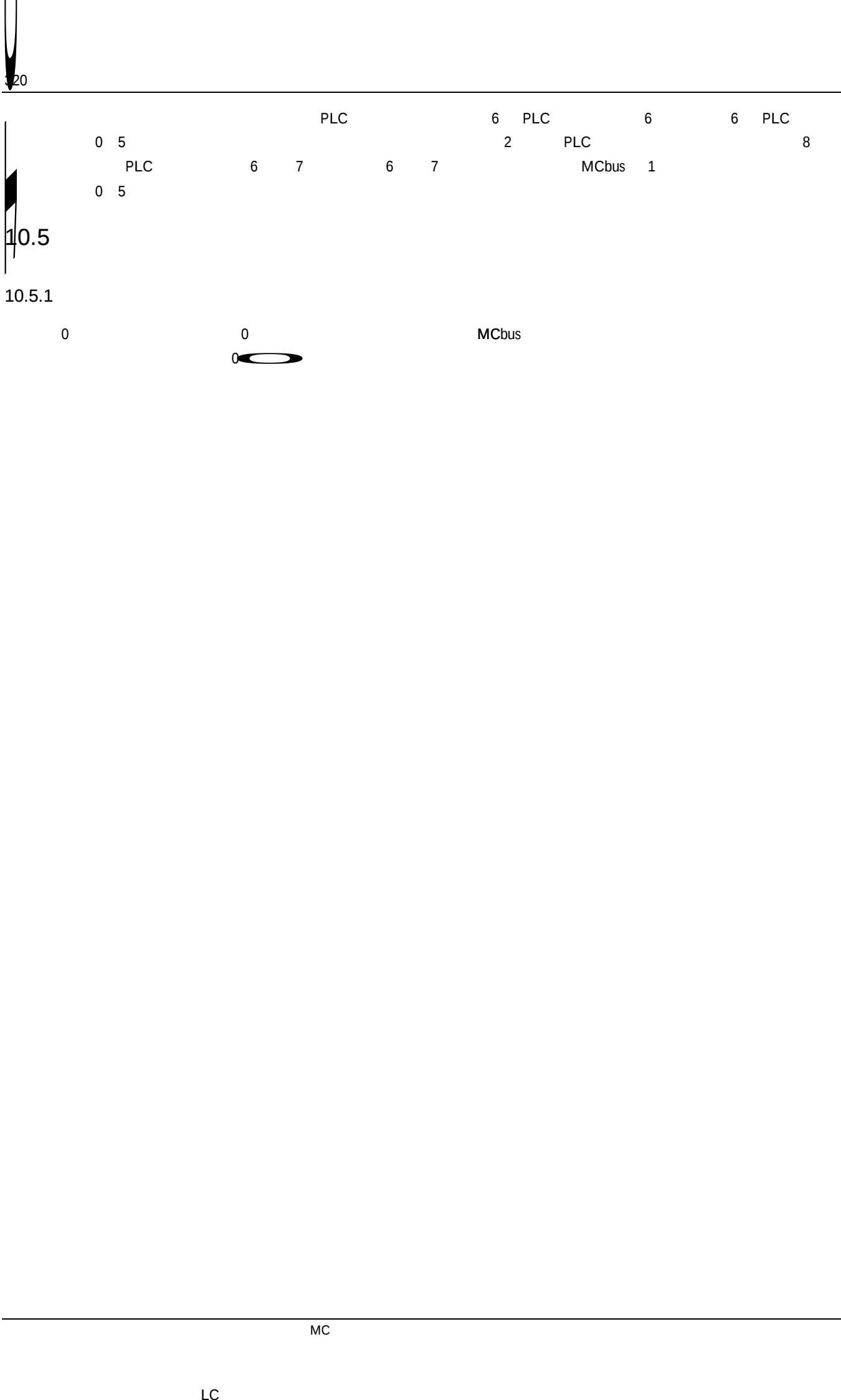
MCbus

MCbus



MCbus0PLC000

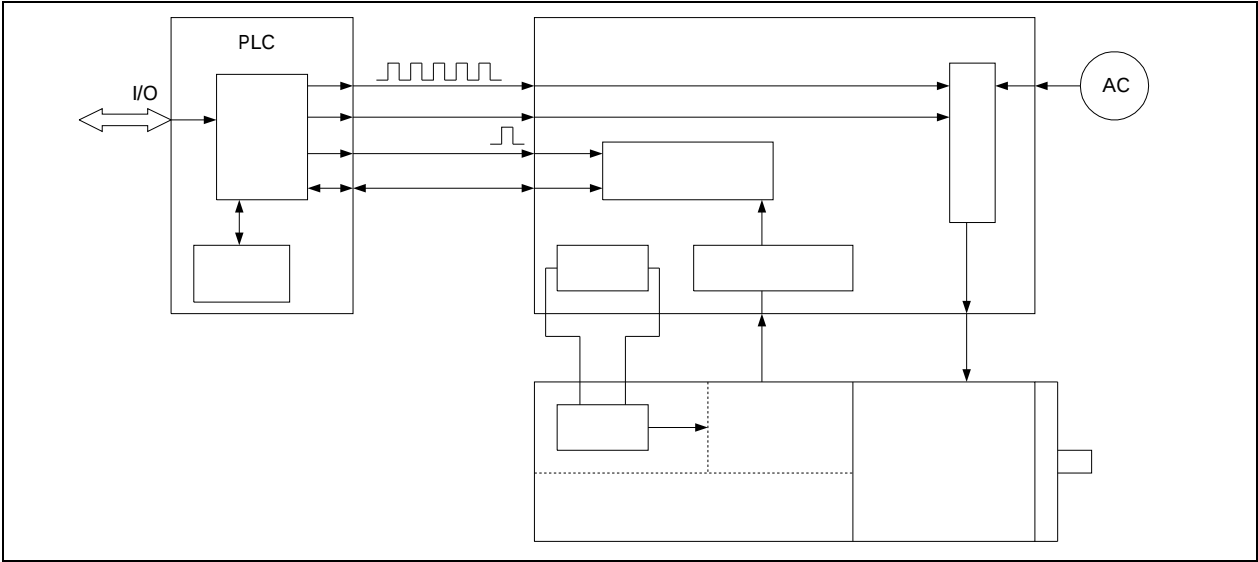




11.1		321
11.1.1		321
11.1.2		322
11.1.3		323
11.2 MC	PLC	323
11.3		325
11.4		326
11.4.1 MC280		326
11.4.2 MC200		338
11.4.3 MC100		341
11.5		342
11.5.1		342
11.5.2		349

11.1

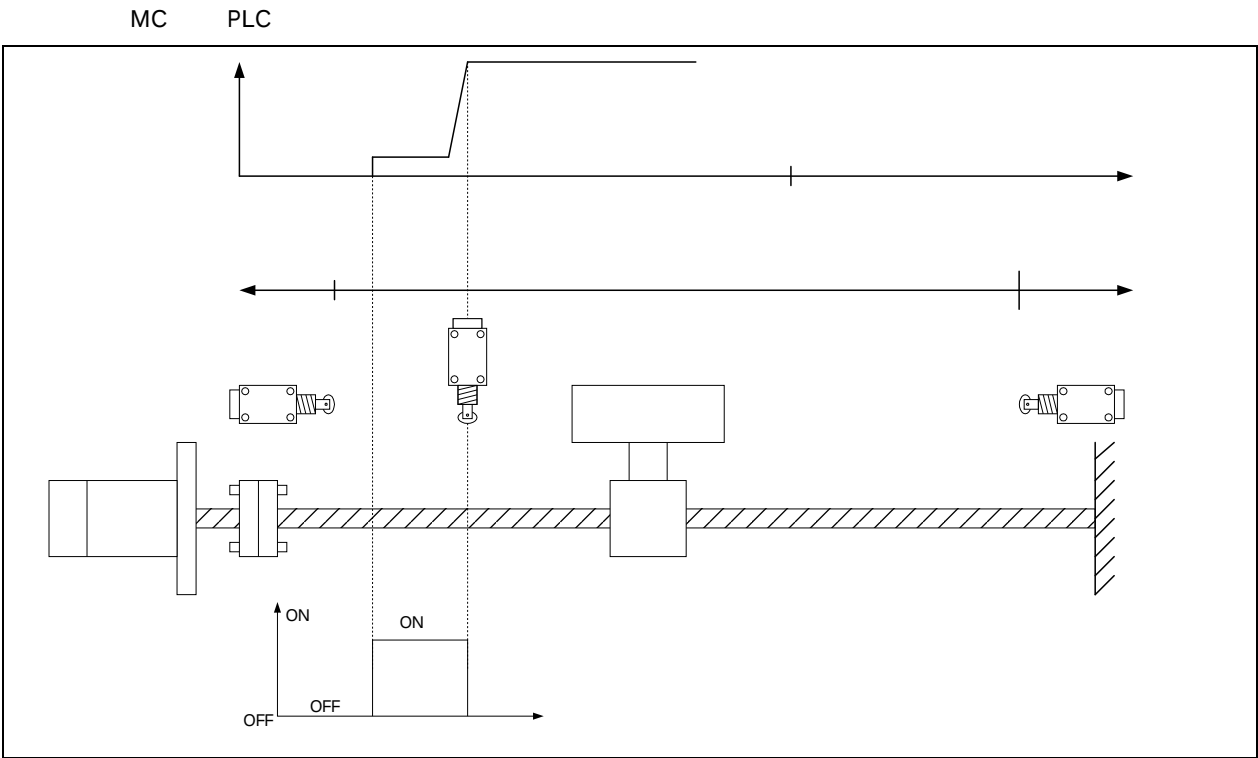
11.1.1



11-1

PLC

PLC

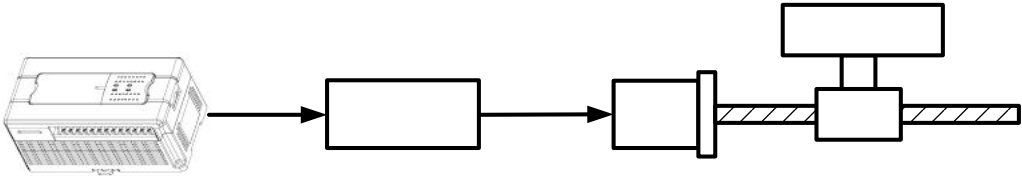


11-2

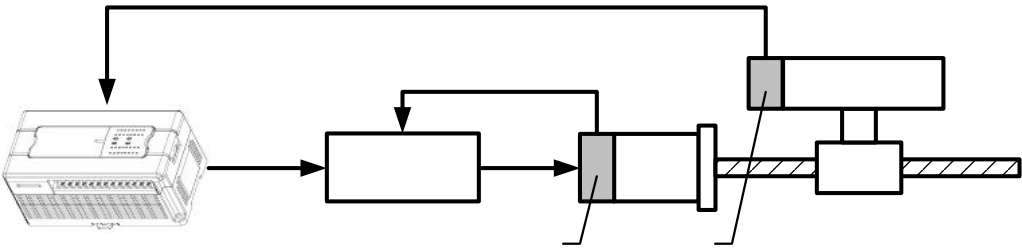
PLC

ZRN

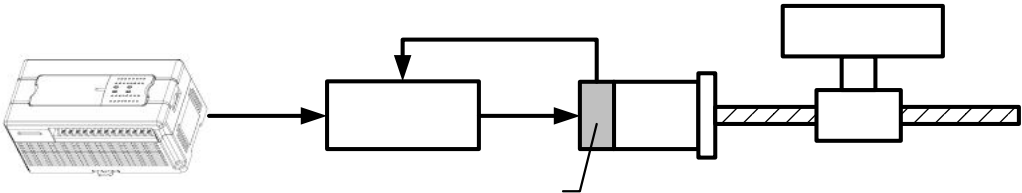
11.1.2



11-3

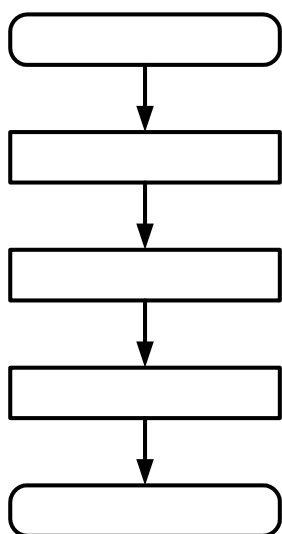


11-4



11-5

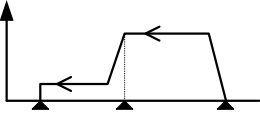
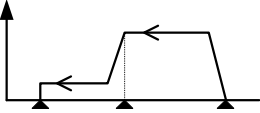
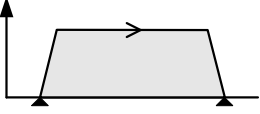
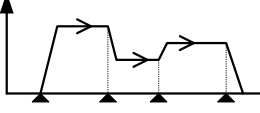
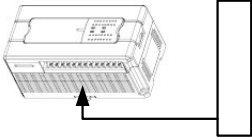
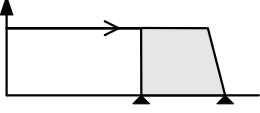
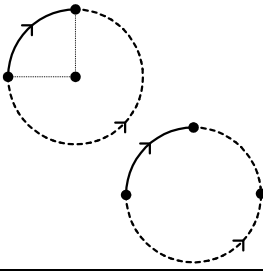
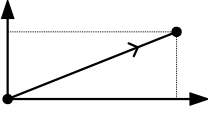
11.1.1.3

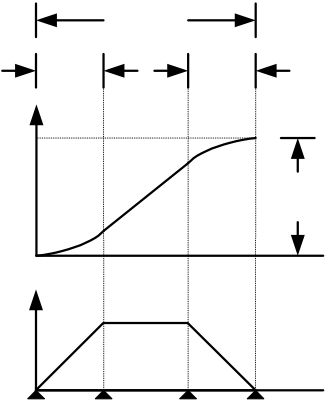
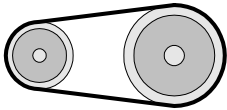


11.2 PLC

MC PLC

11-2 MC PLC

			MC280	MC200	MC100	MC80
DSZR		DOG DOG DOG DOG ON				
ZRN		DOG DOG ON DOG DOG OFF				
DRVI						
DRVA						
PLSV						
ABS						
STOPDV						
CW						
CCW						
LIN						

			MC280	MC200	MC100	MC80
MOVELINK						
GEARBOX						

6.10 IO

11.3

		MC	PLC						
1									
2			1	1	PLC				
3					SD84		SD87		SD85
					SD84		0		0
		0							
	SD84		PLC		SD84	100			
4					SD80/SD82				SD80/SD82
			SD80/SD82				SM82/SM83		
	SD80/SD82		Y0/Y1						
5	SD50/SD52		PLC				SD50/SD52		
							SD80/SD82		
6	SD	MC100	MC200/MC280	SD	MC100				

PLSY PLSR PLS SD

SD SD

SD SD PLSY PLSR PLS PLC

SD

$$F_{min_acc} = \sqrt{\frac{F_{max} \cdot 500}{T}}$$

F_{max} SD85 SD86 T SD87

F_{min_acc}

F 3

- F F F_{max}
- F F_{min_acc} F_{min_acc}
- F F_{min_acc} F_{min_acc} F_{max} F

11.4

11.4.1 MC280

MC280

11-3 MC280-1616BTA8

0	+		Y0	200	X Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	+	
			Y0				
	+		Y0				
			Y1				
	A + B	A	Y0/Y1(A Y1 B)				
		B	Y1/Y0(B Y0 A)				
1	+		Y1	200	X Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7		
			Y1				
	+		Y0				
			Y1				
	A + B	A	Y1/Y0(A Y0 B)				
		B	Y0/Y1(B Y1 A)				
2	+		Y2	200	Y Y0 Y1 Y2 Y3		
			Y2				
	+		Y2				
			Y3				

	A + B	A	Y2/Y3(A Y3 B)		Y4 Y5 Y6 Y7				
		B	Y3/Y2(B Y2 A)						
3	+		Y3	200	Y Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7				
			Y3						
	+		Y2						
			Y3						
	A + B	A	Y3/Y2(A Y2 B)						
B		Y2/Y3(B Y3 A)							
4	+		Y4	100	X /Y /			20	
			Y4						
	PWM								
5	+		Y5	100	X /Y /				
			Y5						
	PWM								
6	+		Y6	100	X /Y /				
			Y6						
	A + B	A	Y6/Y7(A Y7 B)						
		B	Y7/Y6(B Y6 A)						
	PWM								
7	+		Y7	100	X /Y /				
			Y7						
	A + B	A	Y7/Y6(A Y6 B)						
		B	Y6/Y7(B Y7 A)						
	PWM								

11-4 MC280-1616BTA6

0	+		Y0	200	X Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	100		
			Y0					
	+		Y0					
			Y1					
	A + B	A	Y0/Y1(A Y1 B)					
B		Y1/Y0(B Y0 A)						
1	+		Y1	200	X Y0 Y1 Y2 Y3	100		
			Y1					
	+		Y0					
			Y1					

	A +	A	Y1/Y0(A Y0 B)		Y4 Y5 Y6 Y7		
	B	B	Y0/Y1(B Y1 A)				
2	+		Y2	200	Y Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7		
			Y2				
	+		Y2				
			Y3				
	A +	A	Y2/Y3(A Y3 B)				
		B	Y3/Y2(B Y2 A)				
3	+		Y3	200	Y Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7		
			Y3				
	+		Y2				
			Y3				
	A +	A	Y3/Y2(A Y2 B)				
		B	Y2/Y3(B Y3 A)				
4	+		Y4	100	X /Y /	20	
			Y4				
	PWM						
5	+		Y5	100	X /Y /		
			Y5				
	PWM						

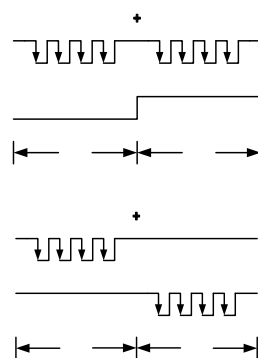
11-5 MC280-1616BTA4

0	+		Y0	200	X Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	100	
			Y0				
	+		Y0				
			Y1				
	A +	A	Y0/Y1(A Y1 B)				
		B	Y1/Y0(B Y0 A)				
1	+		Y1	200	X Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	100	
			Y1				
	+		Y0				
			Y1				
	A +	A	Y1/Y0(A Y0 B)				
		B	Y0/Y1(B Y1 A)				
2	+		Y2	200	Y		
			Y2				

	+		Y2	200	Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	
			Y3			
	A + B	A	Y2/Y3(A Y3 B)			
		B	Y3/Y2(B Y2 A)			
3	+		Y3	200	Y Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	
			Y3			
	+		Y2			
			Y3			
	A + B	A	Y3/Y2(A Y2 B)			
		B	Y2/Y3(B Y3 A)			

11-6 MC200E-1616BTA8

0	+		Y0	200	/	
			Y0			
	+		Y0			
			Y1			
1	A + B	A	Y0/Y1(A Y1 B)	200	/	/
		B	Y1/Y0(B Y0 A)			
	+		Y1			
			Y1			
2	+		Y0	200	/	/
			Y1			
	A + B	A	Y1/Y0(A Y0 B)			
		B	Y0/Y1(B Y1 A)			
3	+		Y2	200	/	/
			Y2			
	+		Y2			
			Y3			
3	A + B	A	Y2/Y3(A Y3 B)	200	/	/
		B	Y3/Y2(B Y2 A)			
	+		Y3			
			Y3			
3	+		Y2	200	/	/
			Y3			
	A + B	A	Y3/Y2(A Y2 B)			
		B	Y2/Y3(B Y3 A)			





	B	B	Y3/Y2(	Y3					
	+		B	Y2 A					
				Y3					
				Y3					
3				Y3	200	/			

		+		Y2				
				Y3				
	A	+	A	Y3/Y2(A Y2 B)				
	B		B	Y2/Y3(B)				



0 1 “ + ” “ + ” 0 1 “ + ”

2-5

0 1 I/O

0 Y0

				RW
--	--	--	--	----

			R/W
SD202	0	10 200000	R/W
SD203	0		R/W
SD204	0		R/W
SD205	0	50 5000 ms	R/W
SD206	0	SM281 N Y Y N	R/W
SD207	0	DSZR	R/W
SD208	0	DSZR	R/W
SD209	0		R/W
SD220	0	PLS	R
1 SD202 SD205			
2 1/10			

1 Y1

			R/W
SM261		Y1	R/W
SM271		Y1 busy ON ready OFF	R
SM71		Y1	R/W
SM310		DSZR/ZRN Y1 CLR	R/W
SM311	Y	DSZR Y1 SD316 N Y Y N Y11	R/W
SM312		DSZR Y1	R/W
SM313		DSZR Y1	R/W
SM314		DSZR Y1	R/W
SM315		DSZR Y1 ON ON OFF ON	R/W
SM316		DSZR Y1 ON ON OFF ON	R/W
SM317		Y1 DVIT	
SM318		DSZR Y1 busy ON ready OFF	R/W
SM319		Y1 DVIT	
SM310 Y11 1 CLR 20ms+1			

1 Y1

			R/W
SD52	1	SD310 SD311 32 SD310	R/W
SD53	1		R/W
SD310	1		R/W
SD311	1		R/W
SD312	1	10 200000	R/W
SD313	1		R/W
SD314	1		R/W
SD315	1	50 5000 ms	R/W
SD316	1	SM311 N Y Y N	R/W
SD317	1	DSZR	R/W

SD318	1	DSZR	R/W
SD319	1		R/W
1 SD312 SD315			
2 1/10			

2 Y2

			R/W
SM262		Y2	R/W
SM272		Y2 busy ON ready OFF	R
SM72		Y2	R/W
SM320		DSZR/ZRN Y2 CLR	R/W
SM321		DSZR Y2 SD326 N Y Y N Y12	R/W
SM322		DSZR Y2	R/W
SM323		DSZR Y2	R/W
SM324		DSZR Y2	R/W
SM325		DSZR Y2 OFF ON ON ON	R/W
SM326		DSZR Y2 OFF ON ON ON	R/W
SM327		Y2 DVIT	
SM328		DSZR Y2 busy ON ready OFF	R/W
SM329		Y2 DVIT	
SM320 Y12 1 CLR			20ms+1

2 Y2

			R/W
SD160	2	SD320 SD321 32 SD320	R/W
SD161	2		R/W
SD320	2		R/W
SD321	2		R/W
SD322	2	10 200000	R/W
SD323	2		R/W
SD324	2	1/10	R/W
SD325	2	50 5000 ms	R/W
SD326	2	SM321 N Y Y N	R/W
SD327	2	DSZR	R/W
SD328	2	DSZR	R/W
SD329	2		R/W
SD222	2	PLS	R
1 SD322 SD325			
2 1/10			

3 Y3

			R/W
--	--	--	-----

R/W
R/W
R/W
R/W
R/W
R/W
R/W
20ms+1

R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W

à 100MHz

SM355		DSZR	Y5		OFF		R/W
		ON		ON	ON		
SM356		DSZR	Y5		OFF		R/W
		ON		ON	ON		
SM358		DSZR	Y5	busy	ON	ready	OFF
	SM350		Y15	1	CLR		20ms+1

5 Y5

							R/W
SD166	5				SD166	SD167	R/W
SD167	5						R/W
SD350	5	SD350	SD351				R/W
SD351	5		32		SD350		R/W
SD352	5						R/W
SD353	5			10	100000		R/W
SD354	5				1/10		R/W
SD355	5			50	5000	ms	R/W
SD356	5	SM351	N	Y	Y	N	R/W
SD357	5	DSZR					R/W
SD358	5	DSZR					R/W
SD359	5	DSZR					R/W
SD225	5	PLS					R
1 SD352 SD355							
2 1/10							

6 Y6

							R/W
SM266		Y6					R/W
SM276		Y6	busy	ON	ready	OFF	R
SM76		Y6					R/W
SM360		DSZR/ZRN	Y6			CLR	R/W
			CLR				
SM361		DSZR	Y6		SD366	N	R/W
	Y	Y N			Y16		
SM362		DSZR	Y6				R/W
SM363		DSZR	Y6				R/W
SM364		DSZR	Y6				R/W
SM365		DSZR	Y6		OFF		R/W
		ON		ON	ON		
SM366		DSZR	Y6		OFF		R/W
		ON		ON	ON		
SM368		DSZR	Y6	busy	ON	ready	OFF
	SM360		Y16	1	CLR		20ms+1

6 Y6

							R/W
SD168	6				SD168	SD169	R/W

			R/W
SD169	6	SD360 SD361	R/W
SD360	6	32 SD360	R/W
SD361	6		R/W
SD362	6	10 100000	R/W
SD363	6		R/W
SD364	6	1/10	R/W
SD365	6	50 5000 ms	R/W
SD366	6	SM361 N Y Y N	R/W
SD367	6	DSZR	R/W
SD368	6	DSZR	R/W
SD369	6		R/W
SD226	6	PLS	R
1 SD362 SD365			
2 1/10			

7 Y7

			R/W
SM267		Y7	R/W
SM277		Y7 busy ON ready OFF	R
SM77		Y7	R/W
SM370		DSZR/ZRN Y7 CLR CLR	R/W
SM371	Y	DSZR Y7 SD376 N Y Y N Y17	R/W
SM372		DSZR Y7	R/W
SM373		DSZR Y7	R/W
SM374		DSZR Y7	R/W
SM375		DSZR Y7 OFF ON ON ON	R/W
SM376		DSZR Y7 OFF ON ON ON	R/W
SM378		DSZR Y7 busy ON ready OFF	R/W
SM370 Y17 1 CLR 20ms+1			

7 Y7

			R/W
SD170	7	SD170 SD171	R/W
SD171	7		R/W
SD370	7	SD370 SD371	R/W
SD371	7	32 SD370	R/W
SD372	7	10 100000	R/W
SD373	7		R/W
SD374	7	1/10	R/W
SD375	7		

			R/W
SD378	7	DSZR	R/W
SD379	7		R/W
SD227	7	PLS	R
1 SD372 SD375			
2 1/10			

11.4.2 MC200

MC200

11-9 MC200

0	+		Y0
			Y0
1	+		Y1
			Y1

0 Y0

			R/W
SM80	Y0	Y0	R/W
SM82	Y0	Y0 busy ON ready OFF	R
SM63	Y0	Y0	R/W
SM280		DSZR/ZRN Y0 CLR	R/W
SM281		DSZR Y0 SD220 Y N Y10	R/W
SM282		DSZR Y0	R/W
SM283		DSZR/DVIT Y0	R/W
SM284		DSZR/DVIT Y0	R/W
SM285		DSZR Y0 ON ON OFF ON	R/W
SM286		DSZR Y0 ON ON OFF ON	R/W
SM287		DVIT Y0 ON ON OFF ON	R/W
SM288		DSZR/DVIT Y0 busy ON ready OFF	R/W
SM289	Y0	DVIT Y0 SD240 X N X0	R/W
SM260		DVIT Y0 Y1 SM289 SM299 SD240	R/W

SM280

Y10 1 CLR

20ms+1

0 Y0

			R/W
SD50	0	SD200 SD201 32 SD200	R/W
SD51	0		R/W
SD200	0		R/W
SD201	0		R/W
SD202	0	10 100000	R/W
SD203	0		R/W
SD204	0	1/10	R/W
SD205	0	50 5000 ms	R/W
SD207	0	DSZR	R/W
SD208	0	DSZR	R/W
SD209	0		R/W
SD220	0	SM281 N Y Y N	R/W
SD240		SM289 N Y Y N 0	R/W
1 SD202 SD205			
2 1/10 1/10			

1 Y1

			R/W
SM81	Y1	Y1	R/W
SM83	Y1	Y1 busy ON ready OFF	R
SM64	Y1	Y1	R/W
SM290		DSZR/ZRN Y1 CLR CLR	R/W
SM291		DSZR Y1 SD230 Y N Y11	R/W
SM292		DSZR Y1	R/W
SM293		DSZR/DVIT Y1	R/W
SM294		DSZR/DVIT Y1	R/W
SM295		DSZR Y1 OFF ON ON ON	R/W
SM296		DSZR Y1 OFF ON ON ON	R/W
SM297		DVIT Y1 OFF ON ON ON	R/W
SM298		DSZR/DVIT Y1 busy ON ready OFF	R/W
SM299	Y1	DVIT Y1 SD240 X N X1	R/W
SM260		DVIT Y0 Y1 SM289 SM299 SD240	R/W
SM290 Y11 1 CLR 20ms+1			

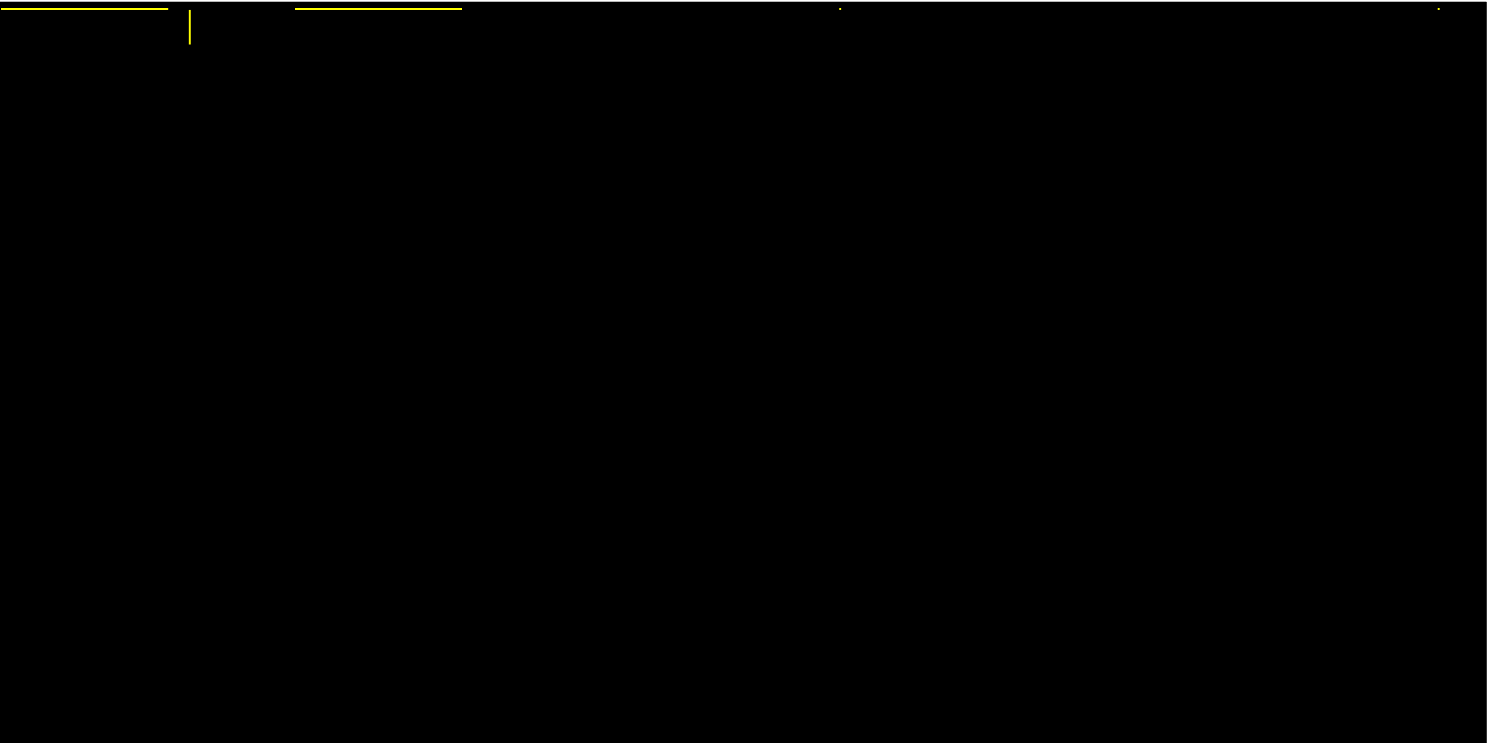
1 Y1

				R/W
SD52	1	SD210 SD211 32 SD210	SD52 SD53	R/W
SD53	1		R/W	
SD210	1		R/W	
SD211	1		R/W	
SD212	1	10 100000		R/W
SD213	1		R/W	
SD214	1	1/10		R/W
SD215	1	50 5000 ms		R/W
SD217	1	DSZR		R/W
SD218	1			R/W
SD219	1		R/W	
SD230	1		N	R/W
SD240			N > 1/10 68 0	R/W
1 SD212 SD215				
2 1/10 1/10				

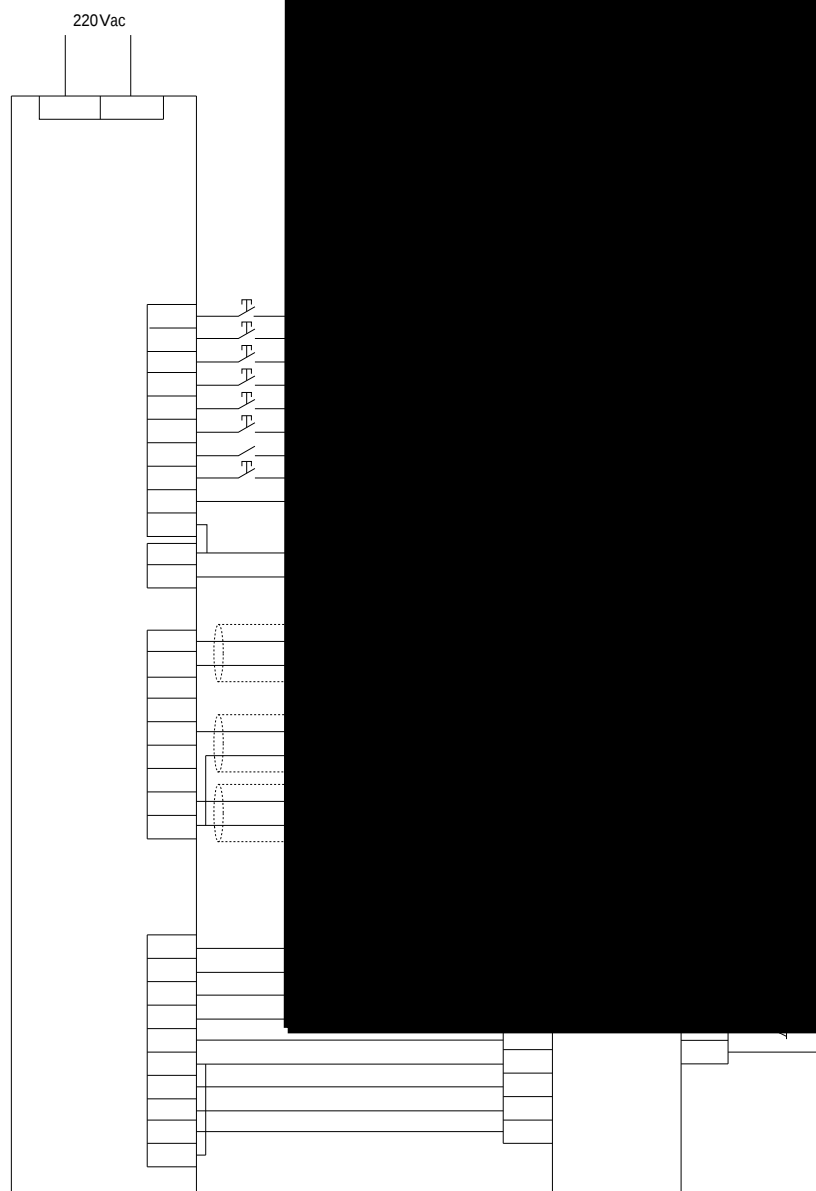
11.4.3 MC100

MC100

11-10 MC100



			R/W
SD50	0	SD80 SD81 32 SD80	R/W
SD51	0		R/W
SD80	0		R/W
SD81	0		R/W
SD52	1	SD82 SD83 32 SD82	R/W
SD53	1		R/W
SD82	1		R/W
SD83	1		R/W
SD84	0 1	1/10	R/W
SD85	0 1	10 100000	R/W
SD86	0 1		R/W
SD87	0 1	50 5000 ms	R/W
SD56	0	PLS	R
SD57	1	PLS	R
1 SD84 SS			

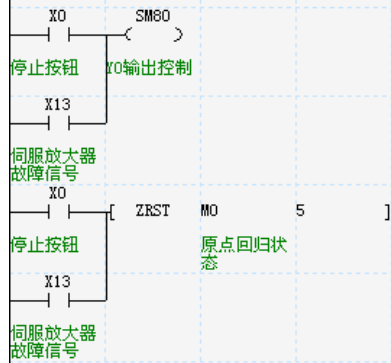


7

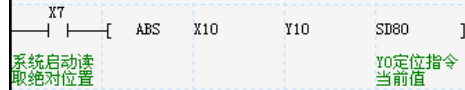
/*上电初始化*/



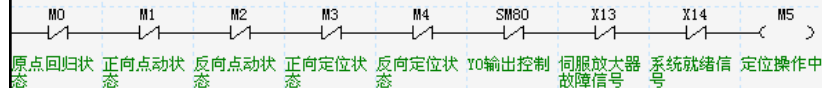
/*故障和停止时停止输出脉冲，并停止所有的定位操作*/



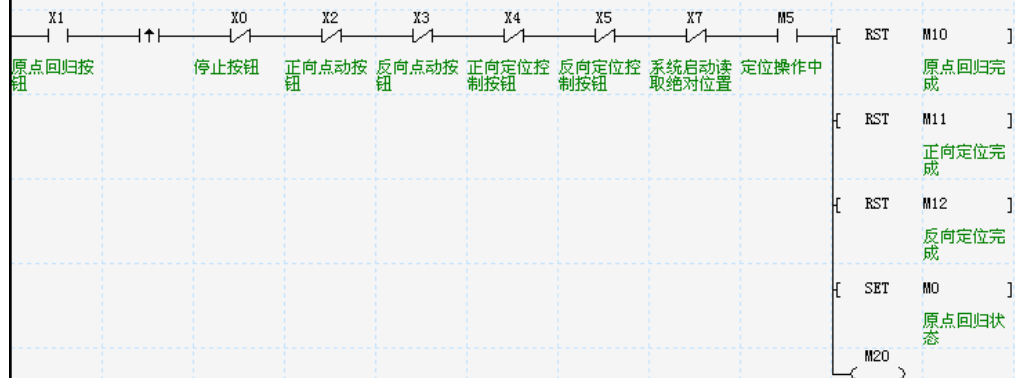
/*绝对位置值读取*/

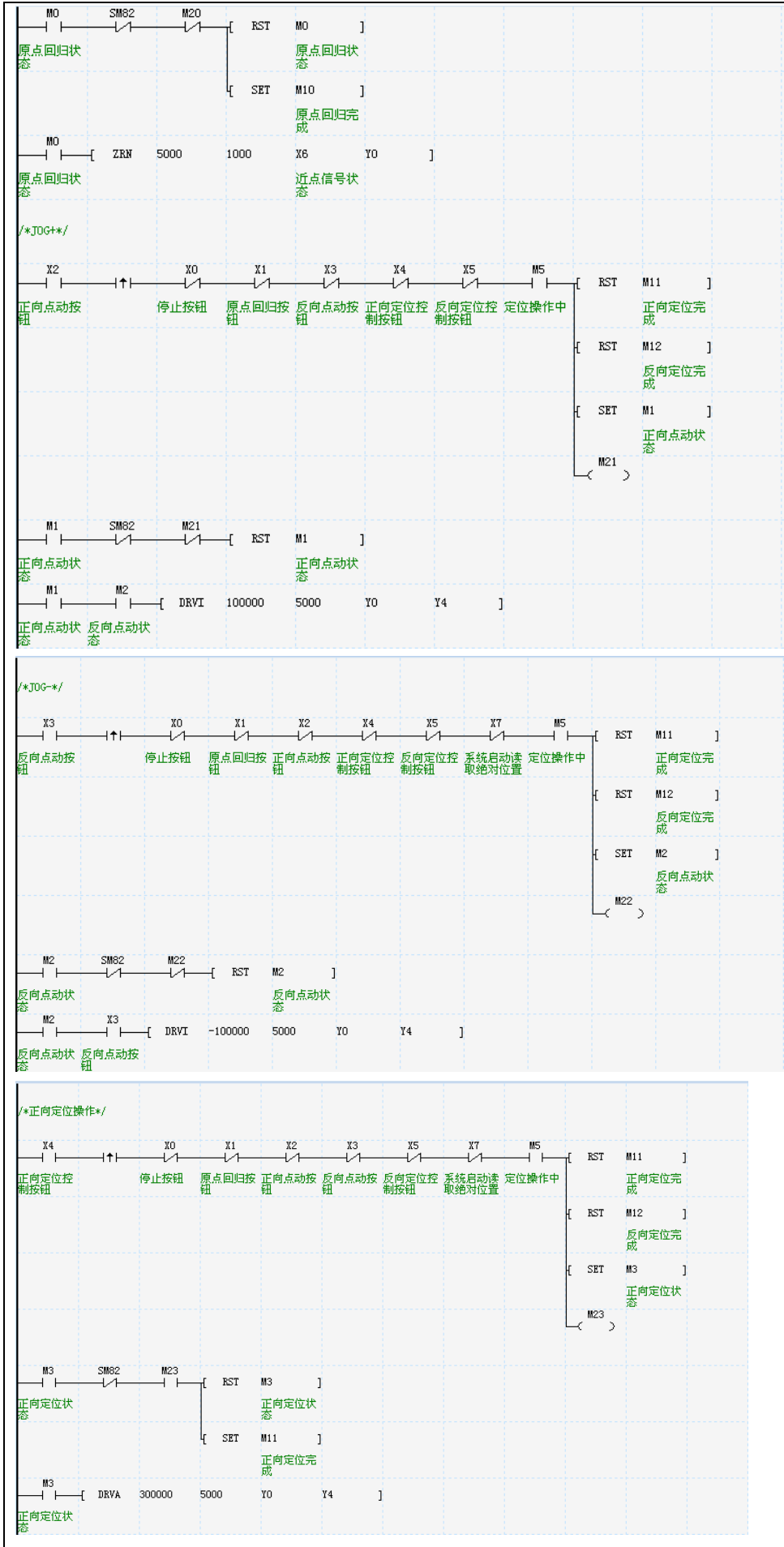


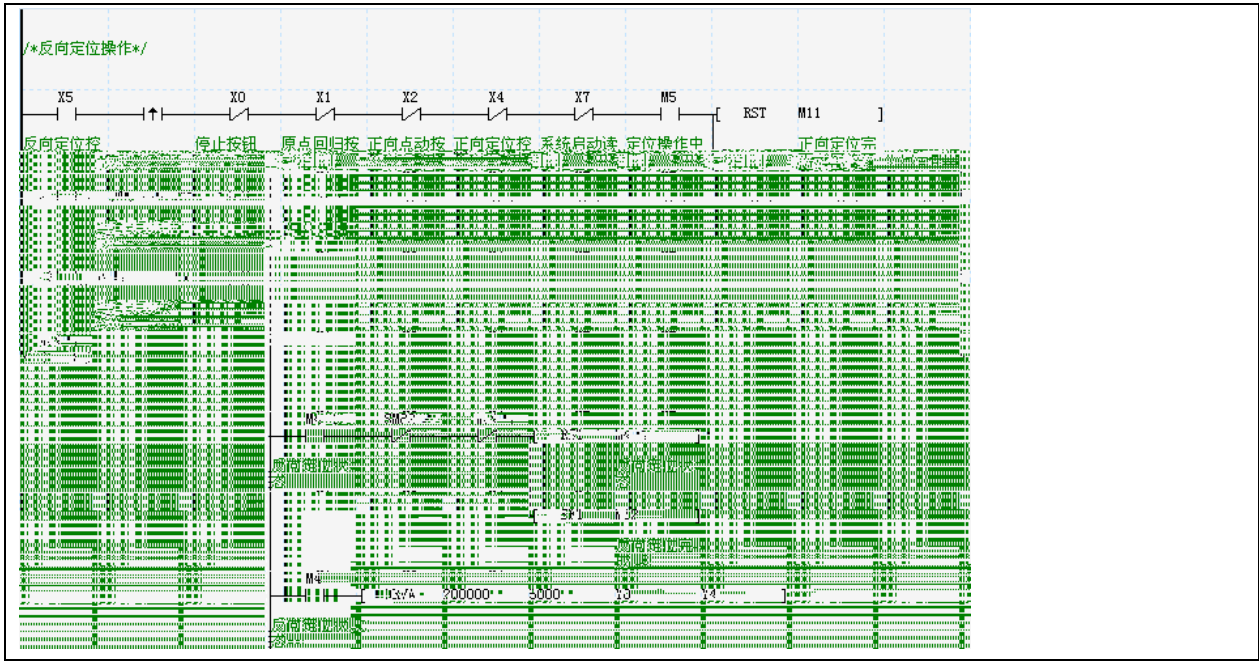
/*检测是否正在进行定位操作。M5为0X表示当前没有进行操作。*/



/*原点回归*/







PLS

PLS

PTO

PTO

X_Builder

->

...

PLS

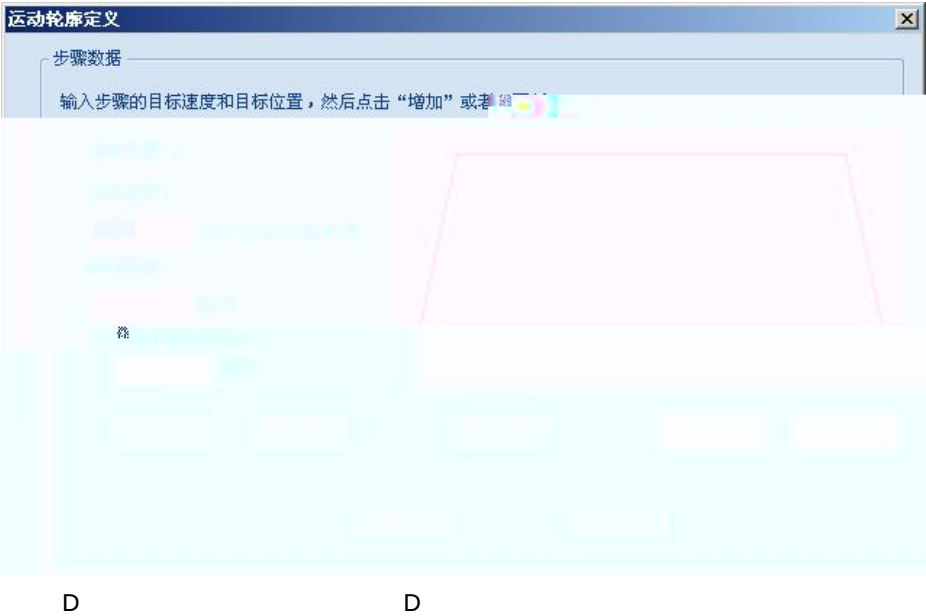




50000Hz 20000Hz

1000 50000 20000 100000 5000 316 0.316

20000 50000 0.316 2 11060



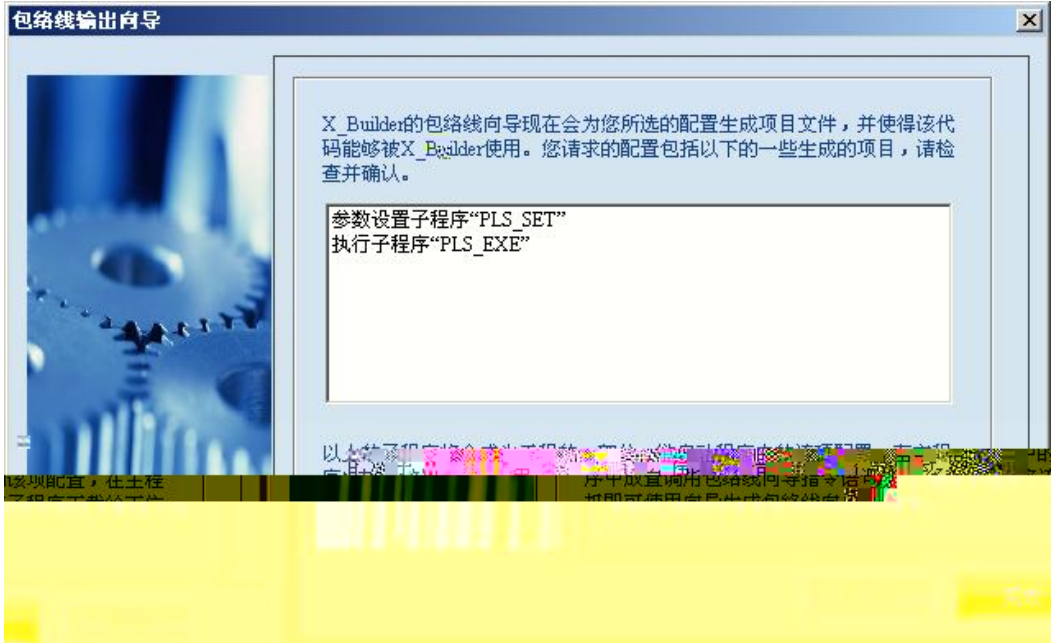


PLS

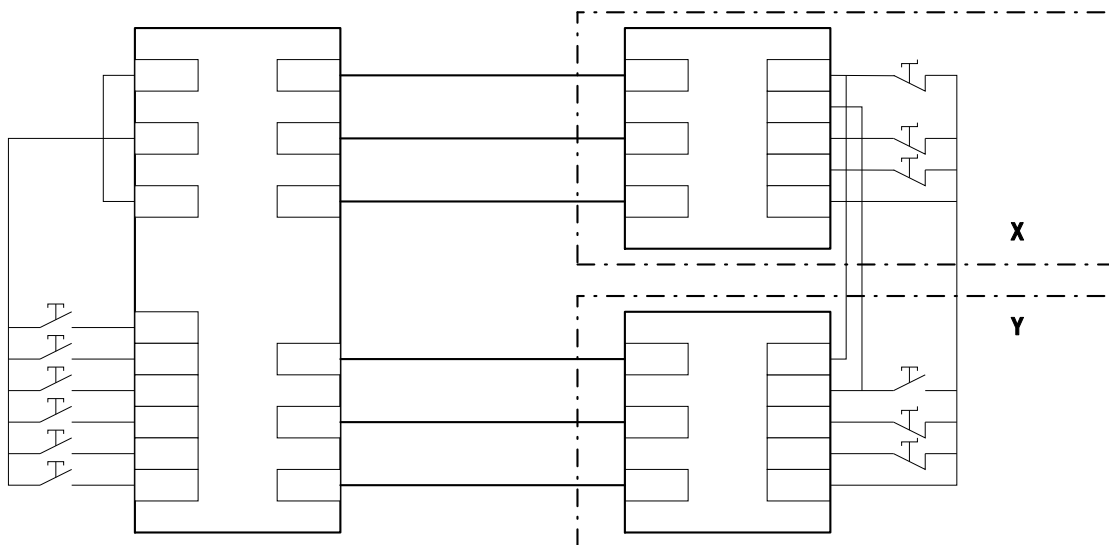
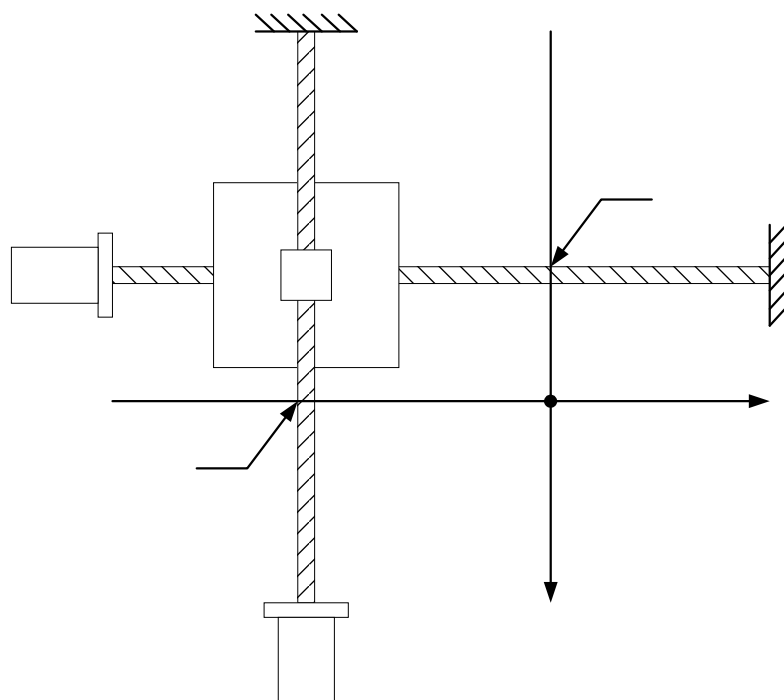
D



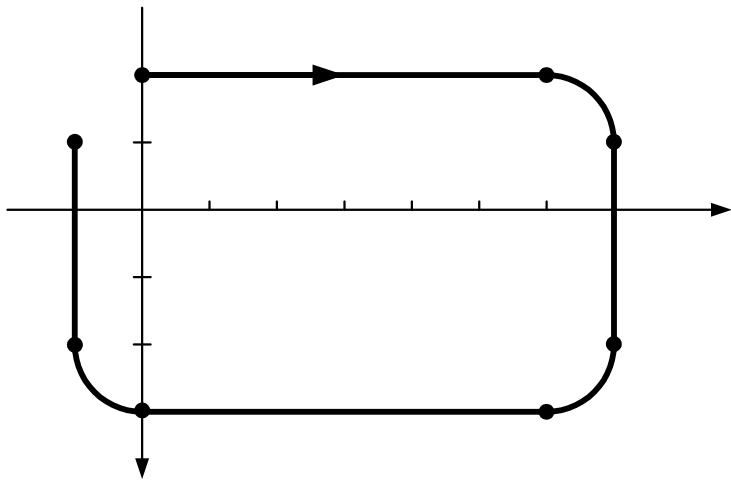
PTO



11.5.2



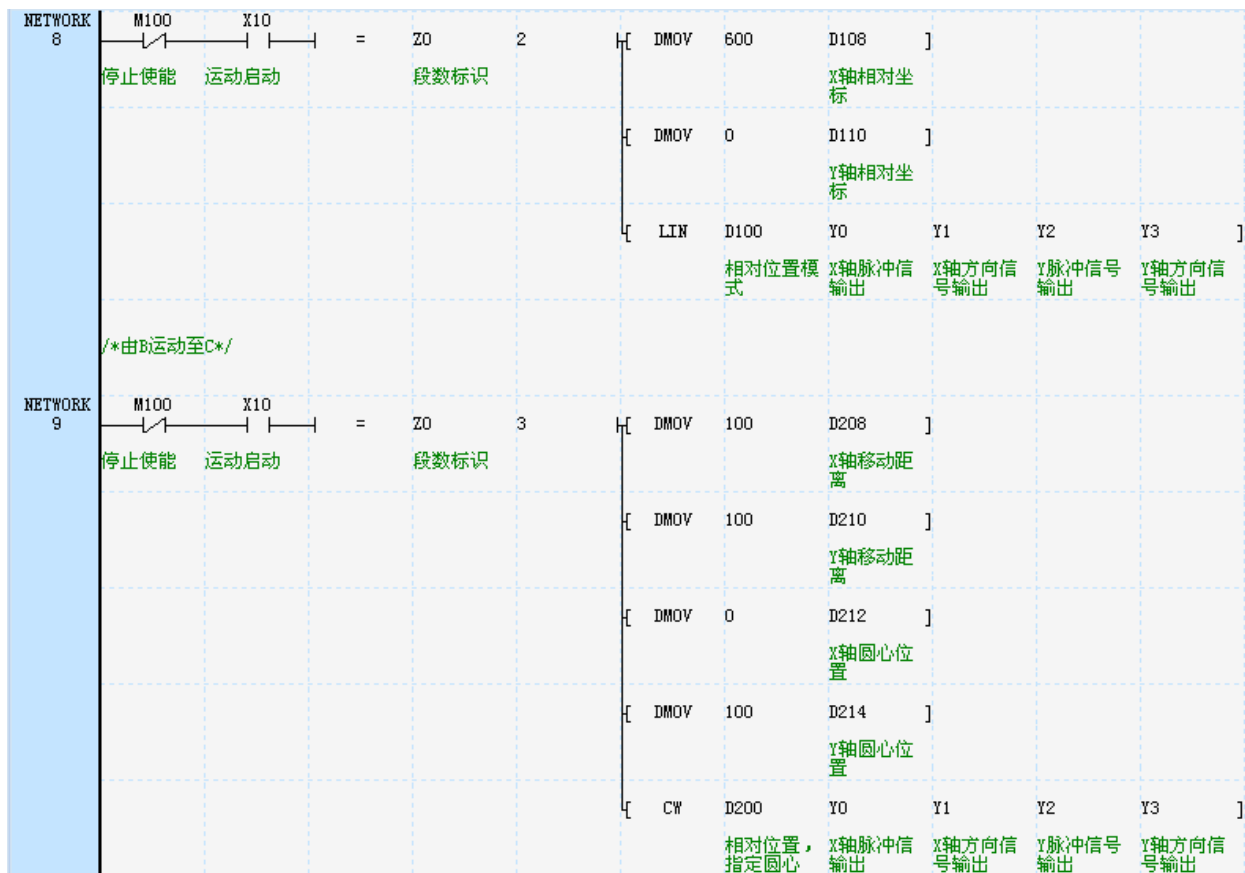
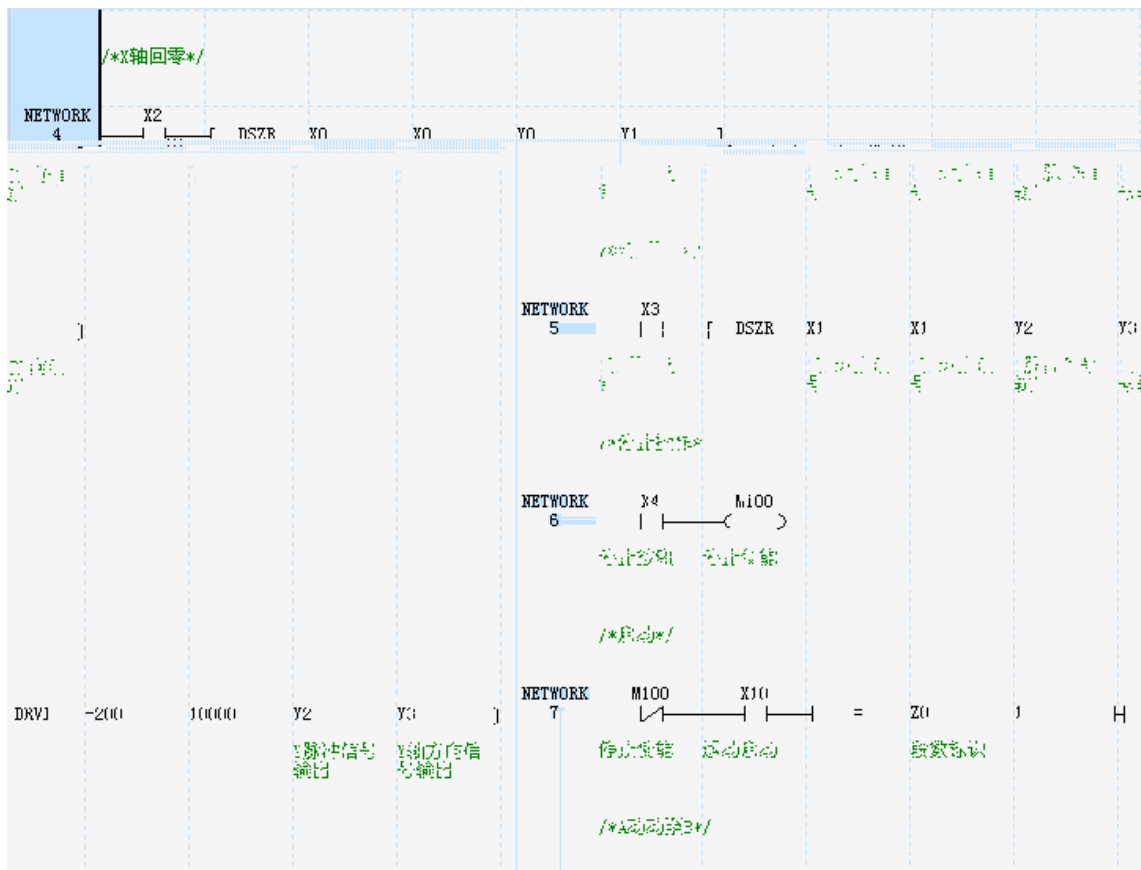
- 1
- 2
- 3

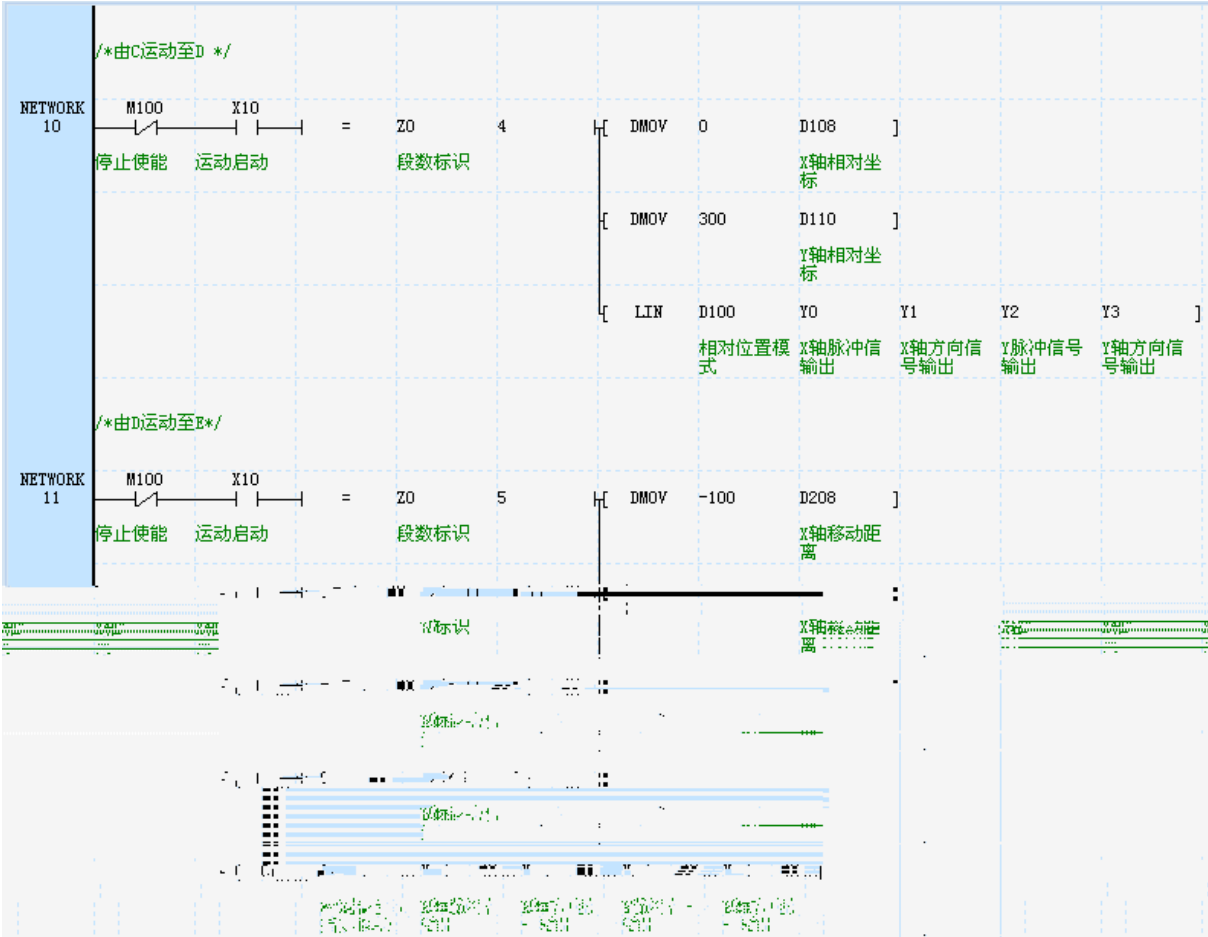


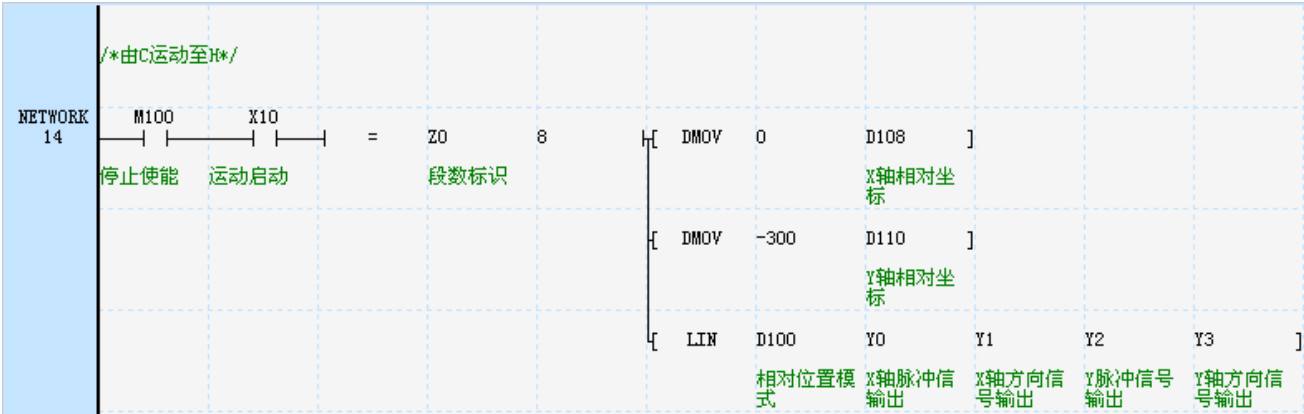
/*初始化运动控制指令相关软元件*/					
NETWORK 0	SM1	[	DMOV	0	D100]
			相对位置模式		
			DMOV	10000	D102]
			直线插补初始速度		
			DMOV	10000	D104]
			直线插补合成速度		
NETWORK 1	SM1	[	DMOV	100	D106]
			直线插补减速速度时间		
			DMOV	0	D108]
			X轴相对坐标		
			DMOV	0	D110]
			Y轴相对坐标		
NETWORK 1	SM1	[	DMOV	0	D200]
			相对位置, 指定圆心		
NETWORK 1	SM1	[	DMOV	10000	D202]
			圆弧插补保留		

	[	DMOV	10000	D204	]	圆弧插补合成速度
	[	DMOV	100	D206	]	保留
	[	DMOV	0	D208	]	X轴移动距离
	[	DMOV	0	D210	]	Y轴移动距离
	[	DMOV	0	D212	]	X轴圆心位置
	[	DMOV	0	D214	]	Y轴圆心位置
	[	MOV	1	Z0	]	段数标识
	[	SET	SM72		]	Y2脉冲输出完成中断
	[	SET	SM69		]	中断使能控制
	[	EI			]	

NETWORK 2	SMO	[	DMOV	200000	SD202	]	Y0最高速度
		[	MOV	10	SD204	]	Y0基底速度
		[	MOV	100	SD205	]	Y0加减速时间
		[	MOV	10	SD207	]	Y0爬行速度
		[	DMOV	2000	SD208	]	Y0回归速度
NETWORK 3	SMO	[	DMOV	200000	SD322	]	Y2最高速度
		[	MOV	10	SD324	]	Y2基底速度
		[	MOV	100	SD325	]	Y2加减速时间
		[	MOV	10	SD327	]	Y2爬行速度
		[	DMOV	2000	SD328	]	Y2回归速度







STOP→RUN



SD SM SM R

1. PLC

			R/W	MC200	MC100	MC280
SM0		RUN STOP	R			
SM1		STOP RUN	R			
SM2			R			
SM3		STOP RUN	R			
SM4		2.4V	R			
SM5		SD05 1" 40ms	R			
SM6	24Vdc	24Vdc 50ms 50ms 24Vdc	R			
SM7		1	R			
SM8			R			
SM9		X ON PLC STOP RUN	R			

2.

			R/W	MC200	MC100	MC280
SM10	10ms	10ms				

5.

			R/W	MC200	MC100	MC280
SM70		1 1-16 0 8	R/W			
SM71		1	R			

6.

			R/W	MC200	MC100	MC280
SM80	Y0	Y0	R/W			
SM81	Y1	Y1	R/W			
SM82	Y0	Y0 busy ON ready OFF	R			
SM83	Y1	Y1 busy ON ready OFF	R			
SM84	PWM	ON OFF	R/W			
SM85		ZRN CLR	R/W			
SM86	Y0	ON PLSY	R/W			
SM87	Y1	ON PLSY	R/W			
SM88		ON	R/W			
SM89	PLSV	ON	R/W			

7.

			R/W	MC200	MC100	MC280
SM90	X0	X0	R/W			
SM91	X1	X1	R/W			
SM92	X2	X2	R/W			
SM93	X3	X3	R/W			
SM94	X4	X4	R/W			
SM95	X5	X5	R/W			
SM96	X6	X6	R/W			
SM97	X7	X7	R/W			
1 STOP RUN HCNT SPD 6.10.9 SPD 6.10.1 HCNT 2 MC100 MC200 X0 X7 SPD HCNT 80k DHSCS DHSCI DHSZ DHSP DHST 30k						

8.

			R/W	MC200	MC100	MC280
SM100	X0 X1 AB 1 /4		R/W			
SM101	X2 X3 AB 1 /4		R/W			
SM102	X3 X4 AB 1 /4		R/W			
SM103	X4 X5 AB 1 /4		R/W			
SM104	X6 X7 AB 1		R/W			

	/4				
--	----	--	--	--	--

9. PORT0

			R/W	MC200	MC100	MC280
SM110	0	XMT 0	R/W			
SM111	0	RCV 0	R/W			
SM112	0		R/W			
SM113	0		R/W			
SM114	0		R			



SM112-SM114 PORT0 MC100 PLC PORT0
 MCbus Modbus FREEPORT SM112-SM114

10. PORT1

			R/W	MC200	MC100	MC280
SM120	1	XMT 1	R/W			
SM121	1	RCV 1	R/W			
SM122	1		R/W			
SM123	1		R/W			
SM124	1		R			



SM122-SM124 PORT1 MC100 PLC
 PORT1 MCbus Modbus FREEPORT SM122-SM124

11. PORT 2

			R/W	MC200	MC100	MC280
SM130	2	XMT 2	R/W			
SM131	2	RCV 2	R/W			
SM132	2		R/W			
SM133	2		R/W			

			R/W	MC200	MC100	MC280
SM134	2		R			



12. Modbus

			R/W	MC200	MC100	MC280
SM135	1 Modbus		R/W			
SM136	1 Modbus		R/W			
SM137	2 Modbus		R/W			
SM138	2 Modbus		R/W			

13. MCbus

			R/W	MC200	MC100	MC280
SM140	0		R			
SM141	1		R			
SM142	2		R			
SM143	3		R			
SM144	4		R			
SM145	5		R			
SM146	6		R			
SM147	7		R			
SM148	8		R			
SM149	9		R			
SM150	10		R			
SM151	11		R			
SM152	12		R			
SM153	13		R			
SM154	14		R			

14.

			R/W	MC200	MC100	MC280
SM172	AD 0	1 AD 0	R/W			
SM173	AD 1	1 AD 1	R/W			
SM174	AD 0	1 0	R/W			
SM175	AD 1	1 0	R/W			
SM178	DA 0	1 DA 0	R/W			

15.

			R/W	MC200	MC100	MC280
SM180			R/W			
SM181	/		R/W			
SM182			R/W			
SM185			R/W			
SM188		1	R/W			

16. ASCII

			R/W	MC200	MC100	MC280
SM186	ASC	0 1 ASCII 1 1 ASCII	R/W			
SM189	SAVER		R			

17.

			R/W	MC200	MC100	MC280
SM190		1 2 STOP RUN 3 4	R			
SM191		1 2	R			
SM192		1 2	R			

18.

			R/W	MC200	MC100	MC280
SM193			R			

19. /

			R/W	MC200	MC100	MC280
SM200	C200	SM2 __ SM2 __ C2 __ C2 __	R/W			
SM201	C201		R/W			
SM202	C202		R/W			
SM203	C203		R/W			
SM204	C204		R/W			
SM205	C205		R/W			
SM206	C206		R/W			
SM207	C207		R/W			
SM208	C208		R/W			
SM209	C209		R/W			
SM210	C210		R/W			
SM211	C211		R/W			
SM212	C212		R/W			
SM213	C213		R/W			
SM214	C214		R/W			
SM215	C215		R/W			
SM216	C216		R/W			
SM217	C217		R/W			
SM218	C218		R/W			
SM219	C219		R/W			
SM220	C220		R/W			
SM221	C221		R/W			
SM222	C222		R/W			
SM223	C223		R/W			
SM224	C224		R/W			
SM225	C225		R/W			
SM226	C226	SM2 __ SM2 __ C2 __ C2 __	R/W			
SM227	C227		R/W			
SM228	C228		R/W			
SM229	C229		R/W			
SM230	C230		R/W			
SM231	C231		R/W			
SM232	C232		R/W			
SM233	C233		R/W			
SM234	C234		R/W			
SM235	C235		R/W			

20.

			R/W	MC200	MC100	MC280
	SM236	C236	R			

SM2 __

				R/W	MC200	MC100	MC280
	SM243	C243		R			
	SM244	C244		R			
	SM245	C245		R			
	SM246	C246		R			
	SM247	C247		R			
	SM301	C301		R			
	SM248	C248		R			
	SM249	C249		R			
	SM250	C250	C2 __ SM2 __	R			
	SM251	C251		R			
	SM304	C304		R			
	SM305	C305		R			
	SM306	C306		R			
	SM252	C252		R			
	SM253	C253		R			
	SM254	C254		R			
	SM255	C255		R/			
	SM256	C256		R/			
	SM257	C257		R/			
	SM258	C258		R/			
	SM259	C259		R/			

21.

			R/W	MC200	MC100	MC280
SM260		Y0 Y1 DVIT Y0 X0 Y1 X1 SD240 4 Y	R/W			
SM261	Y001	Y001	R/W			
SM262	Y002	Y002	R/W			
SM263	Y003	Y003	R/W			
SM264	Y004	Y004	R/W			
SM265	Y005	Y005	R/W			
SM266	Y006	Y006	R/W			
SM267	Y007	Y007	R/W			
SM271	Y001 busy/ready	Y001	R			
SM272	Y002 busy/ready	Y002	R			
SM273	Y003 busy/ready	Y003	R			
SM274	Y004 busy/ready	Y004	R			
SM275	Y005	Y005	R			

			R/W	MC200	MC100	MC200
	busy/ready					
SM276	Y006 busy/ready	Y006				
SM277	Y007 busy/ready	Y007				
SM280		ZRN CLR (Y0) E DSZR/ZRN	R/W			
SM281		SD220 Y N Y2 Y0 DSZR	R/W			
SM282		Y0 DSZR	R/W			
SM283		Y0 DSZR/DVIT	R/W			
SM284		Y0 DSZR/DVIT	R/W			
SM285		Y0 DSZR	R/W			
SM286		Y0 DSZR	R/W			
SM287		Y0 F2+XDVIT	R/W			

			R/W	MC200	MC100	MC280
SM334		Y3 DSZR/DVIT	R/W			
SM335		Y3 DSZR	R/W			
SM336		Y3 DSZR	R/W			
SM338		Y3 DSZR/DVIT	R/W			
SM340		Y4 DSZR/ZRN	R/W			



1 SD50 SD55 STOP → RUN
 2 SD SM SD R

1. PLC

			R/W	MC200	MC100	MC280	
SD00	PLC	10 MC100 20 MC200	R				
SD01		1001 1.001	R				
SD02		12 12k	R				
SD03			R				
SD04		0.1V 3.6V 36	R				
SD05		10ms 10ms 100ms 100ms	R				10 100ms
SD06		4 4 6 6	R				
SD07	I/O		R				
SD08			R				
SD09	10 X0 0 X10 8 15		R			0 15	
SD10	IO		R				
SD11	IO		R				
SD12	IO		R				
SD13							
SD14							
SD15							
SD16							
SD17							
SD18		SM16 0.1ms ,32 0 -- 429496729.5ms	R/W		3.009		
SD19			R/W		3.009		

2. FIFO

			R/W	MC200	MC100	MC280	
SD20	0	5 SD20	R				
SD21	1		R				
SD22	2		R				
SD23	3		R				
SD24	4		R				

6.



9.

			R/W	MC200	MC100	MC280	
SD66	0	1 32767	R/W				1 32767ms
SD67	1	1 32767	R/W				1 32767ms
SD68	2	1 32767	R/W				1 32767ms

1ms

5ms

10.

		R/W	MC200	MC100	MC280	
SD80	Y0	R/W				0
SD81	Y0	R/W				
SD82	Y1	R/W				0
SD83	Y1	R/W				
SD84	ZRN DRVI DRVA	R/W				0
SD85	ZRN DRVI DRVA	R/W				100.000
SD86	ZRN DRVI DRVA	R/W				
SD87	ZRN DRVI DRVA	R/W				100
SD88		R/W				100
SD89		R/W				100

11.

		R/W	MC200	MC100	MC280	
SD100		R				2000 2099
SD101		R				1 12
SD102		R				1 31
SD103		R				0 23
SD104		R				0 59
SD105		R				0 59
SD106		R				0 6
TWR						

12.

0



13. 1

				R/W	MC200	MC100	MC280	
		SD120.0 SD120.2	b2 b1 b0 120.2 000 38,400 001 19,200 010 9,600 011 4,800 100 2,400 101 1,200 110 57,600 111 115,200					
		SD120.3	0 1 1 26CP P P					
		SD120.4	0					

SD120 1 R/W

			R/W	MC200	MC100	MC280	
SD126			R				
SD127			R				
SD128			R				

14. Modbus/MCbus

		R/W	MC200	MC100	MC280	
SD130	0	R/W				MOD 1 32 MCBUS 0 31
SD131	0 /MCbus	R/W				
SD132	0	R/W				
SD133	MCbus 0	R/W				1 13
SD135	1	R/W				MOD 1 32 MCBUS 0 31
SD136	1 /MCbus	R/W				
SD137	1	R/W				0 100
SD138	MCbus 1	R/W				1 13
SD139	Modbus 1	R				

15.

2

			R/W	MC200	MC100	MC280	
SD140	2	SD140.0 SD140.2	b2 b1 b0 000 38,400 001 19,200 010 9,600 011 4,800 100 2,400 101 1,200 110 57,600 111 115,200	R/W			
		SD140.3	0 1 1 2				
		SD140.4	0 1				
		SD140.5	0 1				
		SD140.6	0 8 1 7				
		SD140.7	1 0				
		SD140.8	1 0				
		SD140.9	1 0				
		SD140.10	1 0				
SD140		SD140.11		R/W			
		SD140.12	0 1				
		SD140.13 SD140.15					

			R/W	MC200	MC100	MC280	
SD141			R/W				
SD142			R/W				
SD143		0ms	R/W				0 32767ms
SD144		0ms	R/W				0 32767ms
SD145		0 1 2 3 4 5	R				

Ä

0

		R/W	MC200	MC100	MC280	
SD182	DHST DHSP	R/W				
SD183	DHST DHSP	R/W				
SD184		R/W				

19.

		R/W	MC200	MC100	MC280	
SD191		R				
SD192		R				
SD193	MODBUS (PORT0)	R				
SD194	MODBUS (PORT1)	R				
SD195	MODBUS (PORT2)	R				

20.

			R/W	MC200		
SD196	PORT0	0 5 5ms	R/W	3.009	09	-32767
SD197	PORT1		R/W	3.009	/	
SD198	PORT2		R/W	3.009	/	

21.

			MC200	MC100	
SD200	Y0		R/W		
SD201	Y0		R/W		
SD202	Y0	DRVI DRVA DSZR	R/W	Å	
SD203	Y0	ZRN PLV DRVA DSZR	R/W		
SD204	Y0	ZRN ÉPLSV DRVA DSZR	R/W		
SD205	Y0	ZRN DRVI DRVA DSZR DVIT	R/W		

SD213	Y1 ZRN PLSV DRVI DRVA DSZR DVIT 10 100000	R/W			
SD214	Y1 ZRN PLSV DRVI DRVA DSZR DVIT (1/10)	R/W			
SD215	Y1 ZRN DRVI DRVA DSZR DVIT SD214 SD212 SD213 50ms 5000ms	R/W			
SD217	Y1 DSZR	R/W			
SD218	Y1 DSZR	R/W			
SD219	Y1 DSZR	R/W			
SD220	Y0	R/W			
SD230	Y1	R/W			
SD240		R/W			

				R/W	MC10 0	MC20 0	MC280
SD220		16	0	Y000	R		
SD221		16	0	Y001	R		
SD222		16	0	Y002	R		
SD223		16	0	Y003	R		
SD224		16	0	Y004	R		
SD225		16	0	Y005	R		
SD226		16	0	Y006	R		
SD227		16	0	Y007	R		
SD310		32	0	Y001	R/W		
SD311							
SD312		32	100000(MC280:2 00000)	ZRN,PLSV,DRVI,DRVA DSZR DVIT (10-100000) y1 MC280 10 200000	R/W		
SD313					R/W		
SD314		16	5000(MC280:500)	ZRN,PLSV,DRVI,DRVA DSZR DVIT (1/10) y1	R/W		
SD315		16	1000	ZRN,DRVI,DRVA DSZR DVIT SD314 SD312,SD313 y1 50ms 5000ms	R/W		
SD316		16	0	Y1	R/W		
SD317		16	1000	Y1 DSZR	R/W		
SD318		32	50000	Y1 DSZR	R/W		
SD319					R/W		
SD320							
SD321		32	0	Y002	R/W		
SD322					R/W		
SD323		32	100000(MC280:2 00000)	ZRN,PLSV,DRVI,DRVA DSZR DVIT (10-100000) y2 MC280 10 200000	R/W		
SD324		16	5000(MC280:500)	ZRN,PLSV,DRVI,DRVA DSZR DVIT (1/10) y2	R/W		
SD325		16	1000	ZRN,DRVI,DRVA DSZR DVIT SD324 SD322,SD323 y2 50ms 5000ms	R/W		

					R/W	MC100	MC200	MC280
SD326		16	0	Y2	R/W			
SD327		16	1000	Y2 DSZR	R/W			
SD328		32	50000	Y2 DSZR	R/W			
SD329					R/W			
SD330		32	0	Y003	R/W			
SD331								
SD332		32	100000(MC280:200000)	ZRN,PLSV,DRV,DRVA DSZR DVIT (10-100000) y3 MC280 10 200000	R/W			
SD333					R/W			
SD334		16	5000(MC280:5000)	ZRN,PLSV,DRV,DRVA DSZR DVIT (1/10) y3	R/W			
SD335		16	1000	ZRN,DRV,DRVA DSZR DVIT SD334 SD332,SD333 y3 50ms 5000ms	R/W			
SD336		16	0	Y3	R/W			
SD337		16	1000	Y3 DSZR	R/W			
SD338		32	50000	Y3 DSZR	R/W			
SD339					R/W			
SD340		32	0	Y004	R/W			
SD341					R/W			
SD342		32	200000	ZRN,PLSV,DRV,DRVA DSZR DVIT (10-100000) y4 MC280 10 200000	R/W			
SD343					R/W			
SD344		16	500	ZRN,PLSV,DRV,DRVA DSZR DVIT (1/10) y4	R/W			
SD345		16	1000	ZRN,DRV,DRVA DSZR DVIT SD344 SD342,SD343 y4 50ms 5000ms	R/W			
SD346		16	0	Y4	R/W			
SD347		16	1000	Y4 DSZR	R/W			
SD348		32	50000	Y4 DSZR	R/W			
SD349					R/W			
SD350		32	0	Y005	R/W			
SD351					R/W			
SD352		32	200000	ZRN,PLSV,DRV,DRVA DSZR DVIT (10-100000) y5 MC280 10 200000	R/W			
SD353					R/W			
SD354		16	500	ZRN,PLSV,DRV,DRVA DSZR DVIT (1/10) y5	R/W			
SD355		16	1000	ZRN,DRV,DRVA DSZR DVIT SD354 SD352,SD353 y5 50ms 5000ms	R/W			
SD356		16	0	Y5	R/W			
SD357		16	1000	Y5 DSZR	R/W			

					R/W	MC100	MC200	MC280
SD358		32	50000	Y5 DSZR	R/W			
SD359					R/W			
SD360		32	0	Y006	R/W			
SD361					R/W			
SD362		32	200000	ZRN,PLSV,DRV,DRVA DSZR DVIT (10-100000) y6 MC280 10 200000	R/W			
SD363					R/W			
SD364		16	500	ZRN,PLSV,DRV,DRVA DSZR DVIT (1/10) y6	R/W			
SD365		16	1000	ZRN,DRV,DRVA DSZR DVIT SD364 SD362,SD363 y6 50ms 5000ms	R/W			
SD366		16	0	Y6	R/W			
SD367		16	1000	Y6 DSZR	R/W			
SD368		32	50000	Y6 DSZR	R/W			
SD369					R/W			
SD370		32	0	Y007	R/W			
SD371					R/W			
SD372		32	200000	ZRN,PLSV,DRV,DRVA DSZR DVIT (10-100000) y7 MC280 10 200000	R/W			
SD373					R/W			
SD374		16	500	ZRN,PLSV,DRV,DRVA DSZR DVIT (1/10) y7	R/W			
SD375		16	1000	ZRN,DRV,DRVA DSZR DVIT SD374 SD372,SD373 y7 50ms 5000ms	R/W			
SD376		16	0	Y7	R/W			
SD377		16	1000	Y7 DSZR	R/W			
SD378		32	50000	Y7 DSZR	R/W			
SD379					R/W			

22.

		R/W	MC100	MC200	MC280
SD401	S900-S999	R/W			

23.

		R/W	MC100	MC200	MC280
SD430	1	R/W			
SD431	2	R/W			
SD432	3	R/W			
SD433	4	R/W			
SD434	5	R/W			

Modbus MC100 MC200 MC280

1. Modbus

MC	PLC	0	Modbus	1	Modbus
1	RS485	RS232	RS232	T	
2	RTU	ASCII	ASCII		
3	Modbus	1	31		
4					
5		38	400	19	200 bps
		9	600 bps	4	800 bps
		2	400 bps	1	200 bps
					19200
8	1				
6	2	252	ASII	252	RTU

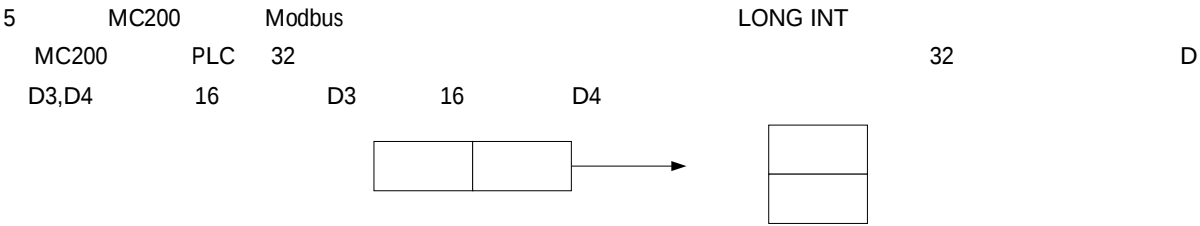
2. Modbus

01 02 03 05 06 08 15 16

		Modicon		
01		0 1:xxxx	Y X M SM S T C	
02		1 5		

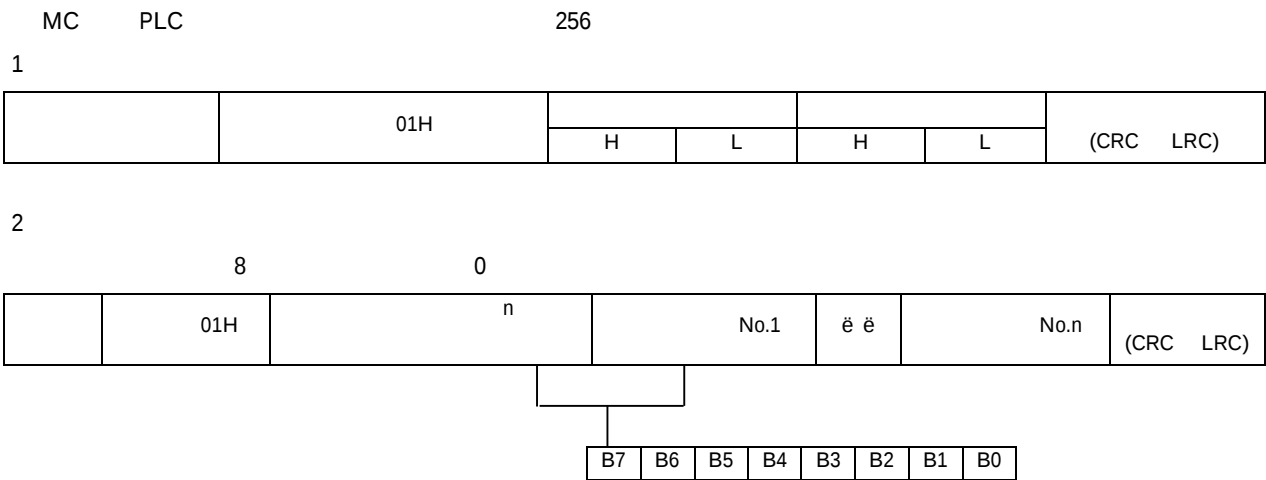
Modbus

	Y0 Y377 8 256	0000 0255	01 05 15	Y0 Y7 Y10 Y17
	X0 X377 8 256	1000 00455 0000 0255	01 05 15 02	
	M0 M10239	2000 4047 12000020191	01 05 15	
	SM0 SM511 S0 S4095	4400 4655 30000-300553 3 6000-7023 31000-30071	01 05 15	% 1 t

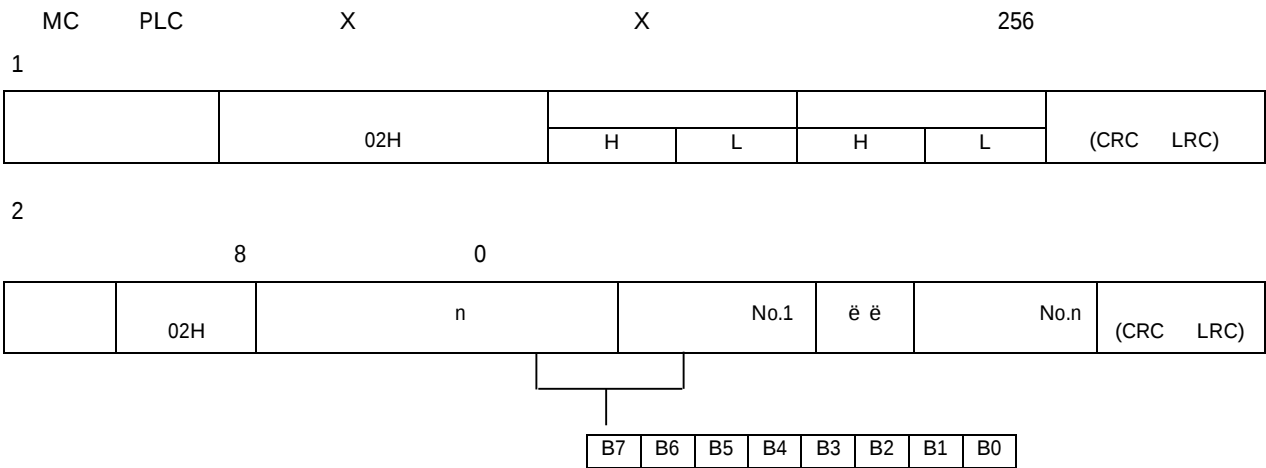


3. Modbus

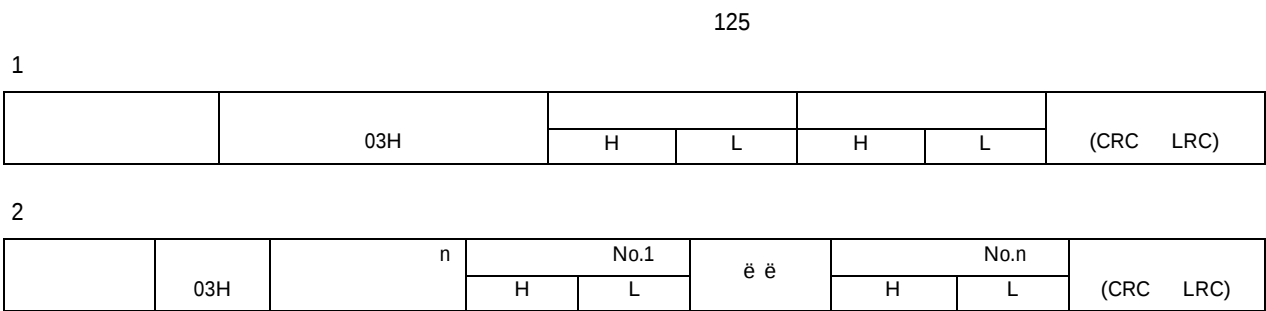
3.1 0x01



3.2 0x02



3.3 0x03



3.8

1.

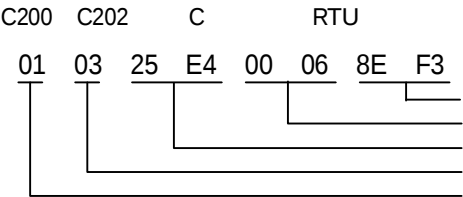
X Y

7010104B0000A BC DA04B0120010X0X90101020000B9FC020000



101CRC2X

1CC200C255C301C306C200C255C301C3060316C



297009701C200970016970016F1A3AP

010325E500045EF225E59701018302C0F1

3010325E40005CEF225E45û7-í™ä™€B-PvHcy`™™tA^7-ÿj½ěñ'™4H`dëó'™™€DvPv00183030131

LONG INT

Modbus

0x01	
0x02	
0x03	
0x10	
0x11	
0x12	/
0x13	
0x14	
0x15	
0x16	
0x17	
0x18	
0x19	
0x1A	CRC/LRC
0x1B	modrw
0x1C	
0x1D	
0x1E	

0x1	
0x2	
0x3	
0x4	
0x5	
0x6	
0x18	
0x20	
0x21	
0x22	

	MC100/MC200		MC80	
	D7940	D7969	D3940	D3969
	D7970	D7999		
	D7800 (MC200)	D7894 (MC200)		
MCbus	D7700	D7763		
MCbus 14-18	D7500	D7755		
MCbus	M1400	M1911		
EROMWR	D6000	D6999		

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

				MC100	MC200	MC280
0						
1 9						
10	SRAM					
11	FLASH					
12						

13

				MC100	MC200	MC280
61						
62						
63						
64			SD20			
65						
66						
67						
68						
69						
70						
71						
72						
73						
74						
75	I/O					
76						
77	PLSR					
78	BFM					
79	ABS					
80	ABS					

MC200

D

MC200

5

PLC

10

EEPROM

D

10

PLC

EEPROM

1	D7800	D7801		D7802		D7803		D7804	D7805-- D7809
2	D7810	D7811		D7812		D7813		D7814	D7815-- D7819
3	D7820	D7821		D7822		D7823		D7824	D7825-- D7829
4	D7830	D7831		D7832		D7833		D7834	D7835-- D7839
5	D7840	D7841		D7842		D7843		D7844	D7845-- D7849
6	D7850	D7851		D7852		D7853		D7854	D7855-- D7859
7	D7860	D7861		D7862		D7863		D7864	D7865-- D7869
8	D7870	D7871		D7872		D7873		D7874	D7875-- D7879
9	D7880	D7881		D7882		D7883		D7884	D7885-- D7889
10	D7890	D7891		D7892		D7893		D7894	D7895-- D7899

ASCII

ASCII HEX		3							
		0	1	2	3	4	5	6	7
4	0	NUL	DLE	SPACE	0	@	P		p
	1	SOH	DC1	!	1	A	Q	a	q
	2	STX	DC2	"	2	B	R	b	r
	3	ETX	DC3	#	3	C	S	c	s
	4	EOT	DC4	\$	4	D	T	d	t
	5	ENQ	NAK	%	5	E	U	e	u
	6	ACK	SYN	&	6	F	V	f	v
	7	BEL	ETB		7	G	W	g	w
	8	BS	CAN	(	8	H	X	h	x
	9	HT	EM	)	9	I	Y	i	y
	A	LF	SUB	*	:	J	Z	j	z
	B	VT	ESC	+	;	K	[	k	{
	C	FF	FS		<	L		l	
	D	CR	GS	-	=	M	]	m	}
	E	SO	RS	.	>	N	^	n	
	F	SI	US	/	?	O		o	DEL



				MC200	MC100	MC80	MC280	
B	BRST		5					203
	BSET		5					203
	BTOW		7					249
C	CALL							87
	CAMBOX		11					245
	CAMTABLE		11					244
	CCITT	CCITT	7					194
	CCW		12					240
	CFEND		1					85
	CIRET		1					86
	CJ		3					85
	COS	COS	7					110
	CRC16	CRC16	7					195
	CSRET		1					87
	CTR	16	5					75
	CTU	16	5					75
	CMP		7	*		*		213
	CW		12					239
D	DADD		10					101
	DBAND		9					218
	DBCD	32 BCD	7					119
	DBIN	32 BCD	7					120
	DBITS	ON	6					198
	DCMP<		7					152
	DCMP<=		7					152
	DCMP<>		7					152
	DCMP=		7					152
	DCMP>		7					152
	DCMP>=		7					152
	DCNT	32	7					76
	DDMC		4					104
	DDIV		10					102
	DMC		3					100
	DEG	->	7					115
	DMCO		5					197
	DFLT		7					117
	DFMOV		9					90
	DFROM		10					139
	DGBIN	32	7					122
	DGRY	32	7					121
	DHSCI		10					158
	DHSCR		10					160
	DHSCS		10					157
	DHSP		10					164
	DHSPI		10					159
	DHST		10					162
	DHSZ		13					161
	DI		1					86
	DINC		4					103

LDR>

LD>

7

				MC200	MC100	MC80	MC280	
	ORD<=	OR<=	7					209
	ORD<>	OR<>	7					209
	ORD=	OR=	7					209
	ORD>	OR>	7					209
	ORD>=	OR>=	7					209
	ORI		1					65
	ORR<	OR>	7					212
	ORR<=	OR<=	7					212
	ORR<>	OR<>	7					212
	ORR=	OR=	7					212
	ORR>	OR>	7					212
	ORR>=	OR>=	7					212
	OUT		1					65
	OUT Sxx	SFC	3					71
P	PID	PID	9					174
	PLS		7					170
	PLSR		10					168
	PLSV		8					230
	PLSY		9					167
	POWER		10					111
	PUSH		7					92
	PWM	PWM	7					173
R	PLSB		12					171
	RAD	->	7					114
	RADD		10					106
	RAMP		12					177
	RCL	16	7					132
	RCR	16	7					131
	RCV	RCV	7					193
	RDIV		10					108
	REF	I/O	5					142
	REFF		3					142
	RET	SFC	1					72
	RLCNV		12					125
	RMOV		7					89
	RMUL		10					107
	RND		3					253
	RNEG		7					109
	ROL	16	7					131
	ROR	16	7					130
	RSQT		7					108
	RST		1					69
	RST Sxx	SFC	3					71
	RSUB		10					107
	RSUM		9					112
	RVABS		7					109
	RCMP		9	*		*		214
	SCL		7					219
	SEG	7	5					122
	SER		9					220
	SET		1					69

					MC200	MC100	MC80	MC280	
	SET Sxx	SFC	3						71
	SFTL		9						137
	SFTR		9						136
	SHL	16	7						135
	SHR	16	7						134
									109
									166
									99
									71
									154

H P †(H -i 8vdP †(H -i 8w&E D b b...`4€Q• P †(H6-i ;P 6!f(V €Q•

				MC200	MC100	MC80	MC280	
W	WAND		7					127
	WDT		1					86
	WINV		5					128
	WOR		7					127
	WSFL		9					96
	WSFR		9					95
	WTOB		7					247
	WXOR		7					127
X	XCH		5					91
	XMT	XMT	7					192
Z	ZONE		9					218
	ZRN		11					229
	ZRST		5					196
	ZSET		5					197
* MC200								

				MC200	MC100	MC80	MC280	
	LD		1					63
	LDI		1					63
	AND		1					64
	ANI		1					64
	OR		1					64
	ORI		1					65
	OUT		1					65
	SET		1					69
	RST		1					69
	ANB		1					66
	ORB		1					66
	INV		1					68
	NOP		1					69
	MPS		1					67
	MRD		1					67
	MPP		1					67
	MC		3					70
	MCR		1					70
	EU		2					68
	ED		2					68
	TON		5					73
	TOF		5					74
	TMON		5					74
	TONR		5					73
	CTU	16	5					75
	CTR	16	5					75
	DCNT	32	7					76
	LBL		3					84
	CJ		3					85
	CALL							87
	CSRET		1					87
	CFEND		1					85
	CIRET		1					86
	FOR		3					83
	NEXT		1					83
	WDT		1					86
	STOP		1					86
	EI		1					86
	DI		1					86

					MC200	MC100	MC80	MC280	
SFC	STL	SFC	3						71
	SET Sxx	SFC	3						71
	OUT Sxx	SFC	3						71
	RST Sxx	SFC	3						71
	RET	SFC	1						72
	MOV		5						88
	DMOV		7						88
	RMOV		7						89
	BMOV		7						89
	SWAP		3						91
	XCH		5						91
	DXCH		7						92
	FMOV		7						90

					MC200	MC100	MC80	MC280	
I/O	HCNT		7						155
	DHSCS		10						156
	DHSCR		10						159
	DHSCI		10						158
	DHSZ		13						161
	DHST		10						162
	DHSP		10						164
	SPD	SPD	7						166
	PLSY		9						167
	PLSR		10						168
	PLSB		12						171
	PWM	PWM	7						173
	PLS		7						173
	RAMP		12						177
	HACKLE ABSD		12 9	M&					178

					MC200	MC100	MC80	MC280	
	TRD		3						147
	TWR		3						148
	TADD		7						

				MC200	MC100	MC80	MC280	
	AND<>	AND<>	5					205
	ANDD<>	AND<>	7					208
	ANDR<>	AND<>	7					211
	OR=	OR=	5					206
	ORD=	OR=	7					209
	ORR=	OR=	7					212
	OR>	OR>	5					206

				MC200	MC100	MC80	MC280	
	BLD	LD	5					199
	BLDI	LDI	5					200
	BAND	AND	5					200
	BANI	ANI	5					201
	BOR	OR	5					201
	BORI	ORI	5					202
	BSET		5					203
	BRST		5					203
	BOUT		5					202
	MC200/100/80/280	MC200/100/80/280	8					182
	XMT	XMT	7					192
	RCV	RCV	7					193
MODRW	MODBUS		14	*		*		184

				MC200	MC100	MC80	MC280	
	STRMOV		5					228
	RND		3					253
	DUTY		7					253
* MC200								